DØSMT

DØ Silicon Microstrip Tracker for runIIa

- Design
- Production
- Assembly
- Readout
- Installation
- Commissioning/Operation
- Some results

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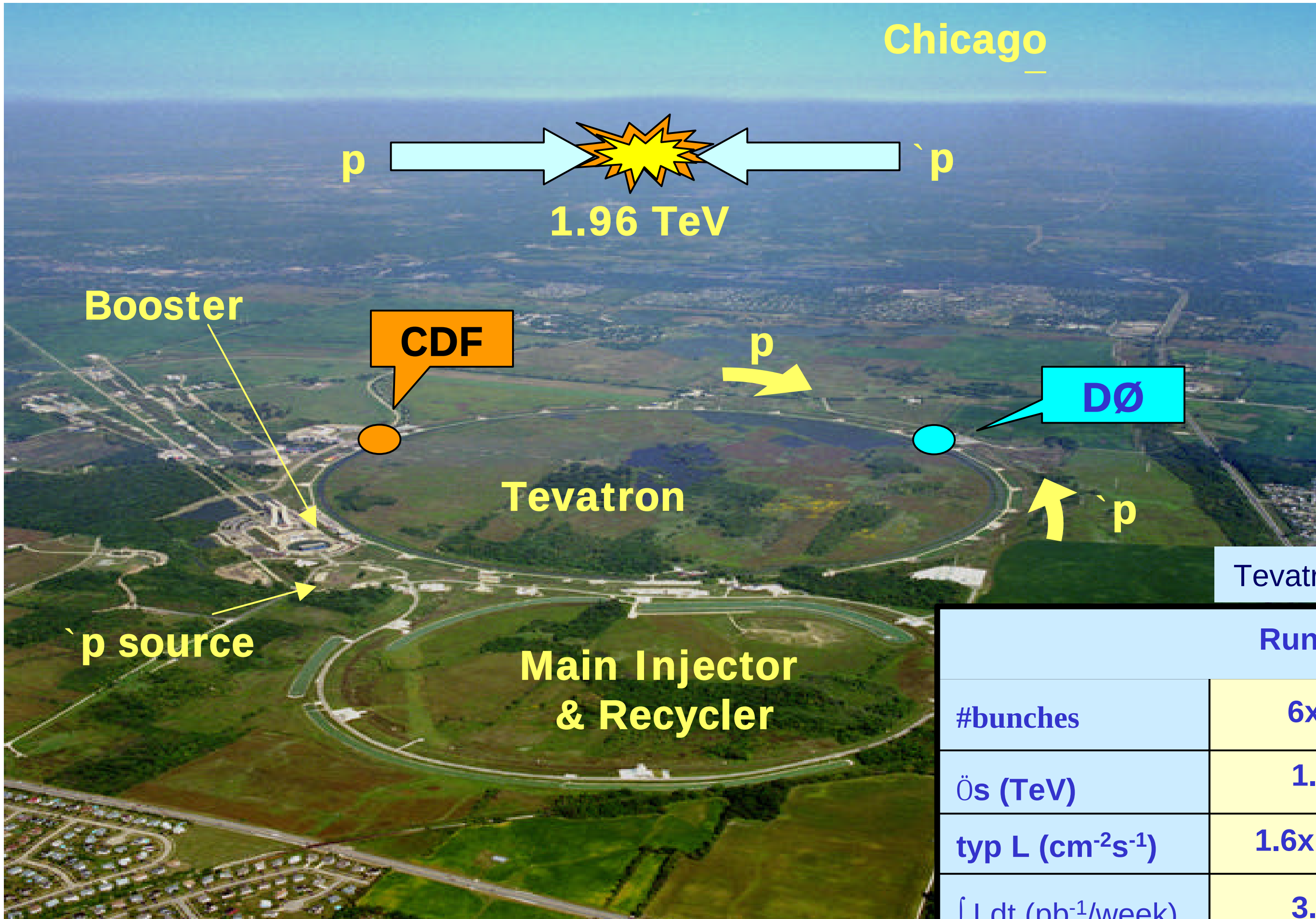
Vertex2002 - Hawaii, November 4, 2002

Fermilab Tevatron

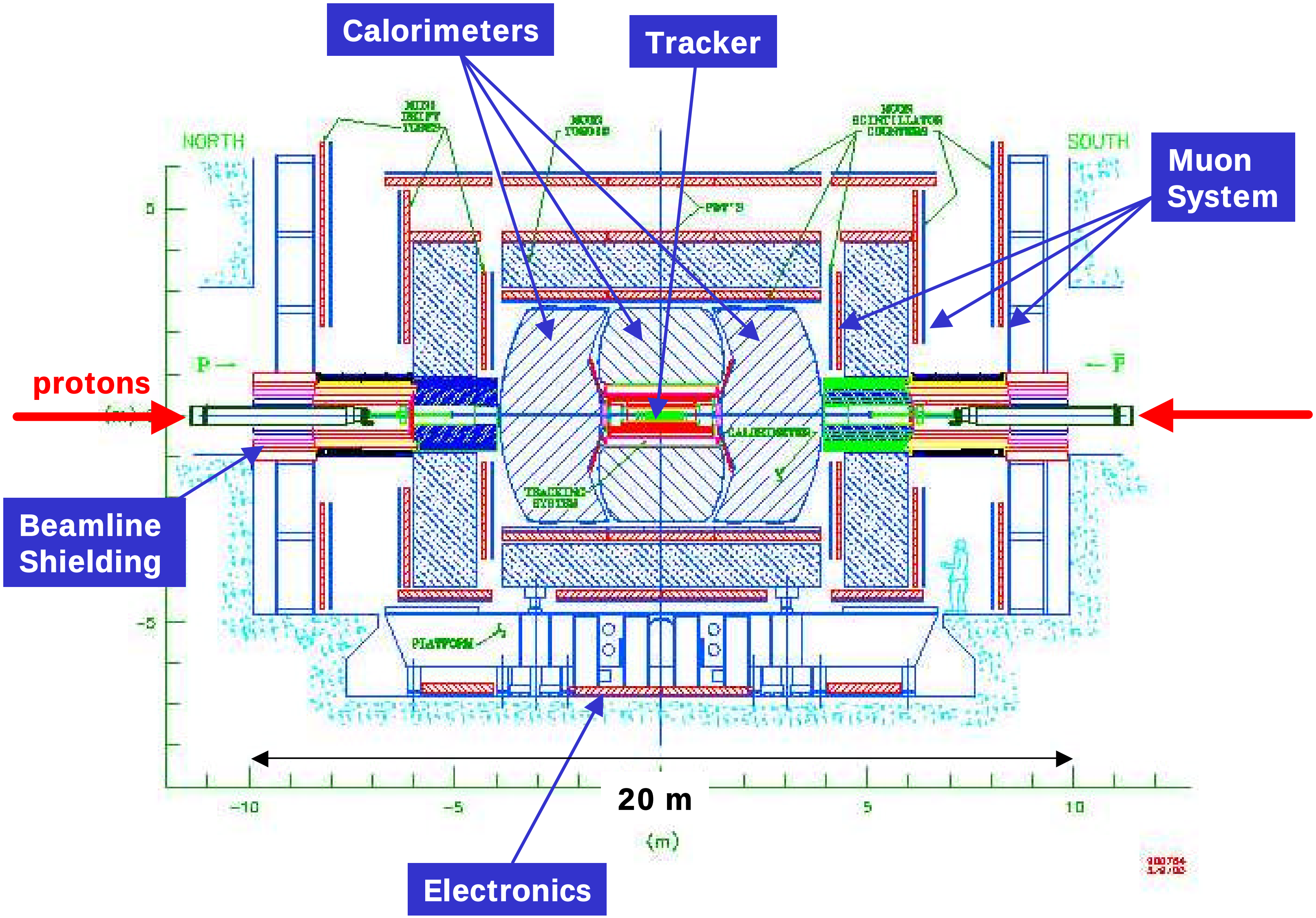


Tevatron upgrade

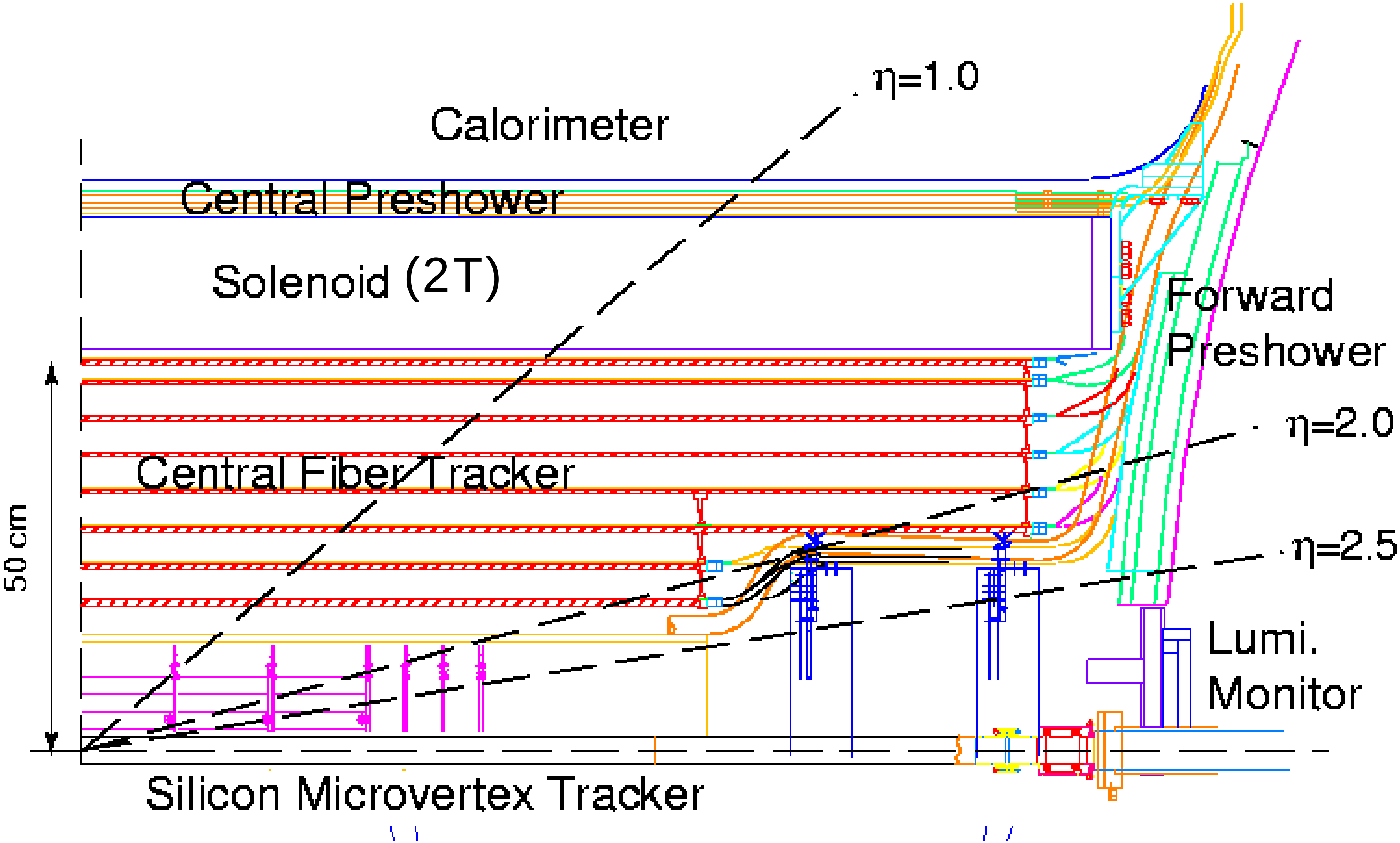
	Run 1B	Run 2A	Run 2B
#bunches	6x6	36x36	140x103
Ös (TeV)	1.8	1.96	1.96
typ L ($cm^{-2}s^{-1}$)	$1.6x10^{30}$	$8.6x10^{31}$	$5.2x10^{32}$
∫ Ldt (pb^{-1}/week)	3.2	17.3	105
bunch xing (ns)	3500	396	132
interactions/xing	2.5	2.3	4.8

Run 1 → Run 2A → Run 2B
0.1 fb^{-1} → 2 fb^{-1} → 15 fb^{-1}

The DØ Detector

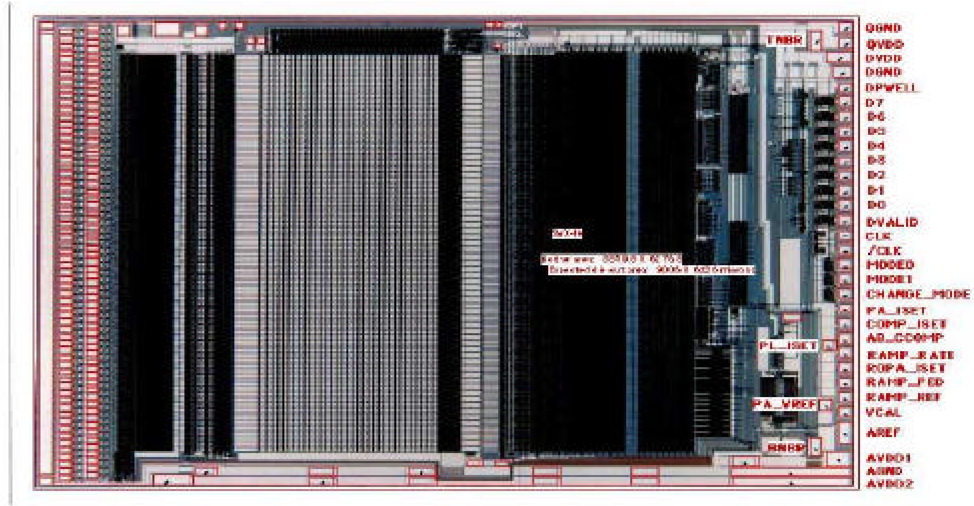


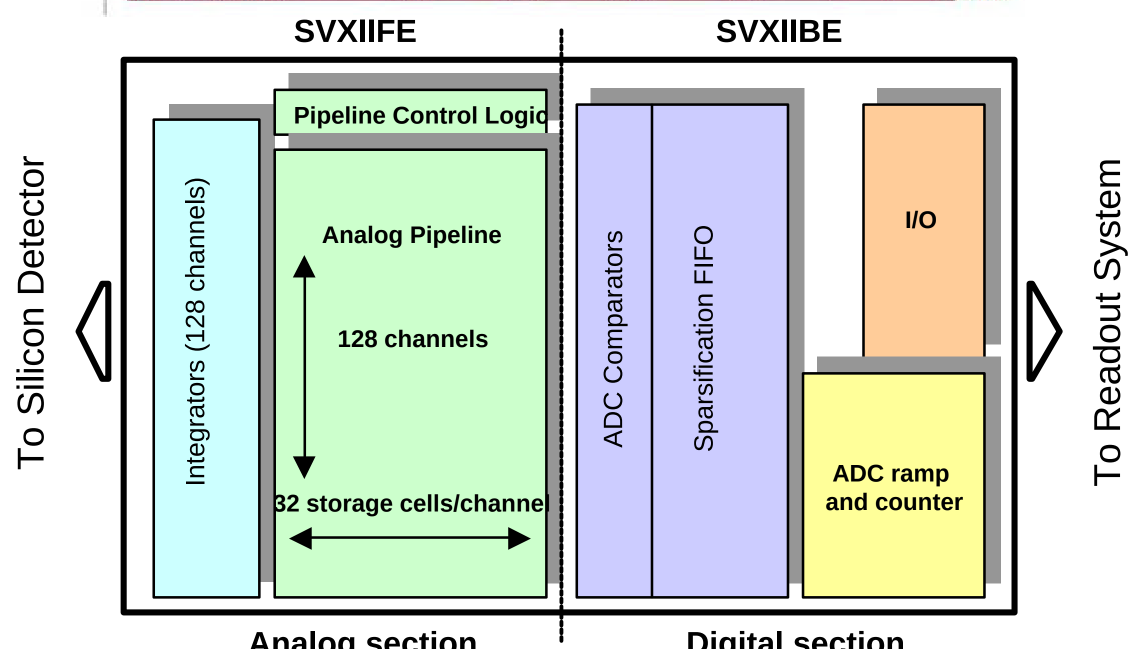
Run IIa SMT Design



SVXIIe chip

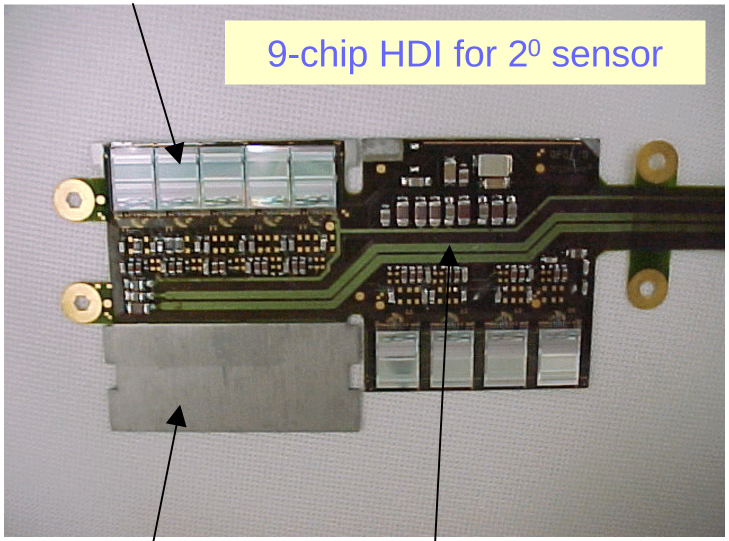
- 1.2 um CMOS amplifier/analog delay/ADC chip fabricated in the UTMC rad hard process
- Designed by LBL/FNAL
- Some features:
  - 128 channels
  - 32 cell pipeline/channel
  - 8-bit Wilkinson ADCs
  - Sparsification
  - 53 MHz readout
  - 106 MHz digitization
  - 6.4 x 9.7 mm2
  - ~ 85,000 transistors
  - noise: 490e + 50e/pF



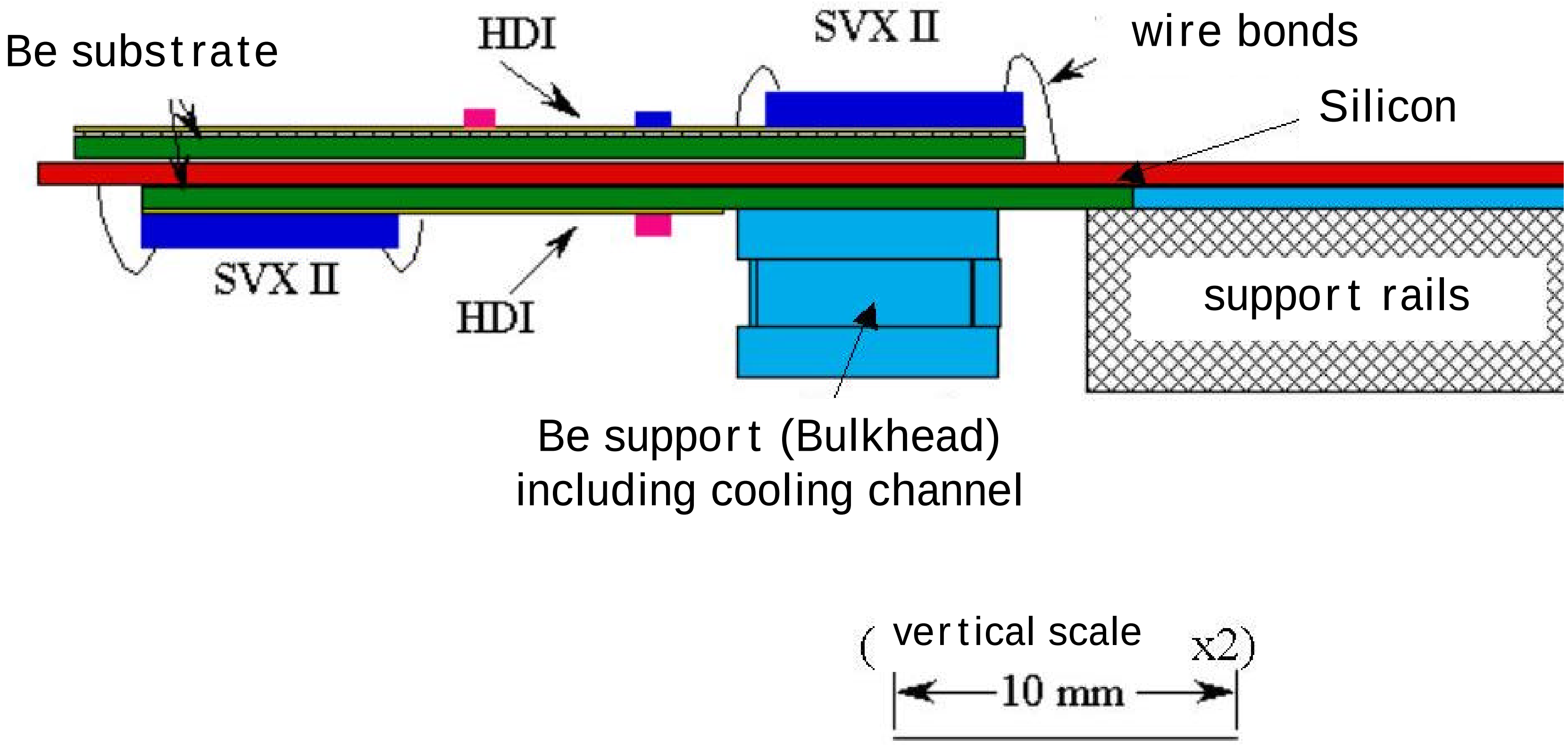


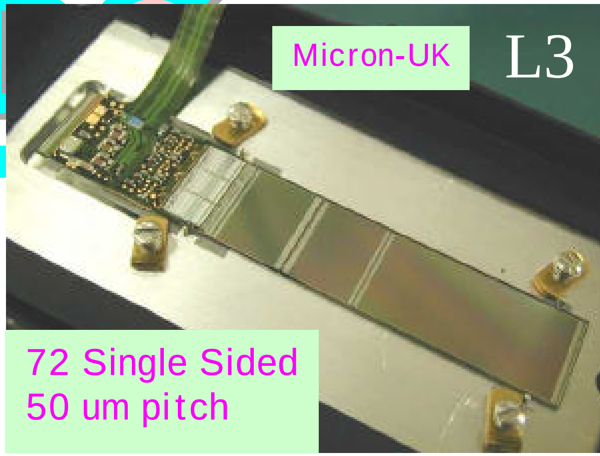
High Density Interconnect

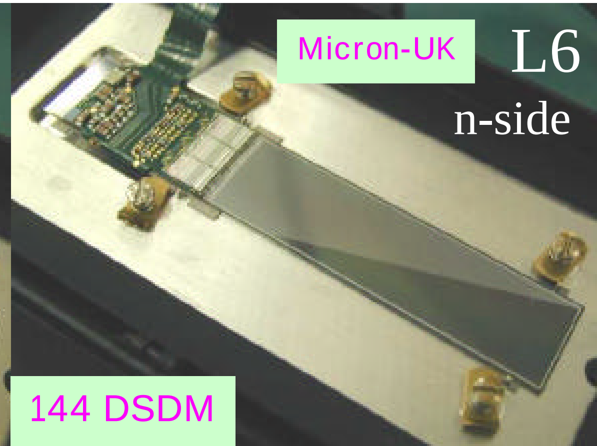
- **Kapton based flex circuits with 0.2 mm pitch for chip mounting**
- **Laminated to Beryllium substrate and glued to Silicon sensor**
- **Connects Sensor to SVXII chips and SVXII chips to flex circuit via wire bonds (Al wedge bonding)**
- **Connects to a Low Mass Cable which carries the signals out of the interaction region**

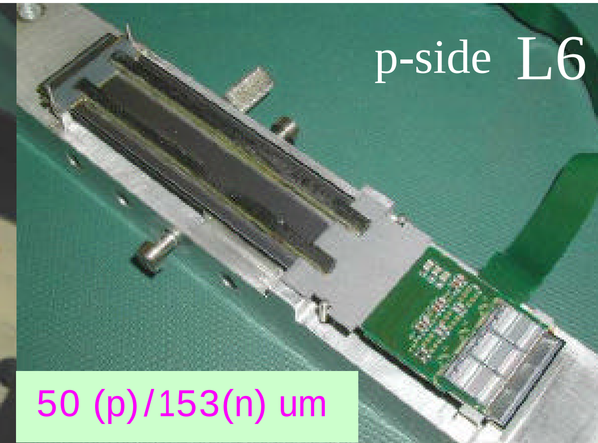


Production: ladder design

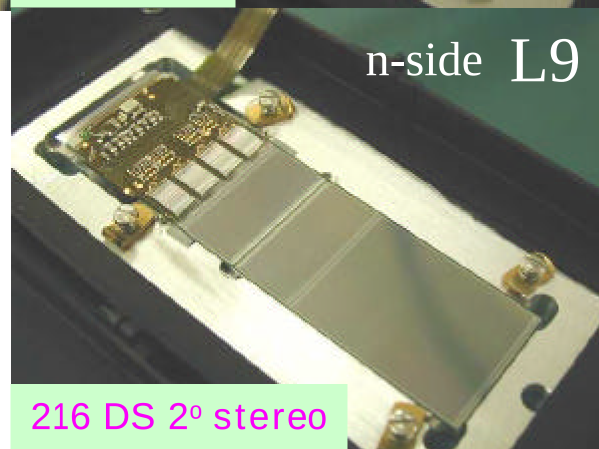


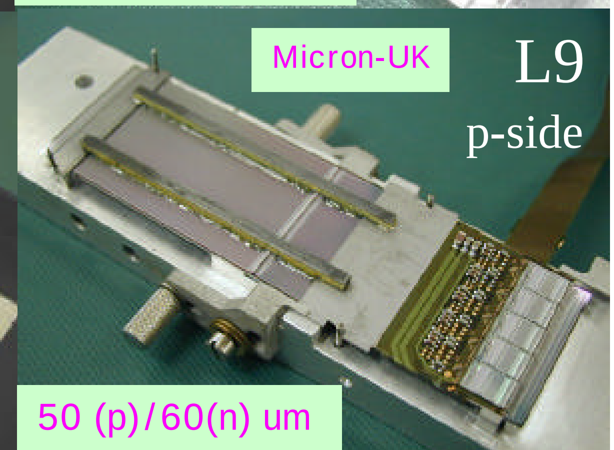


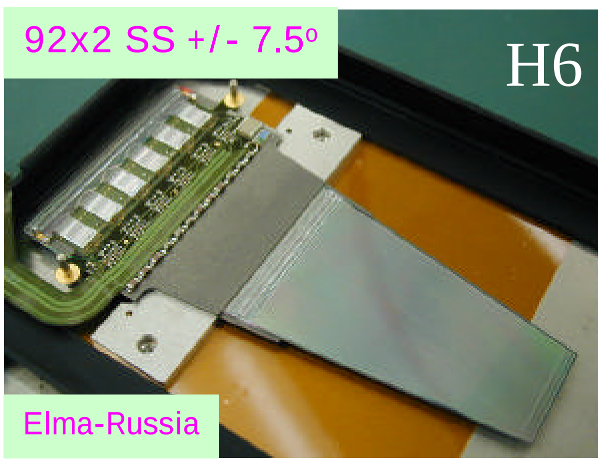


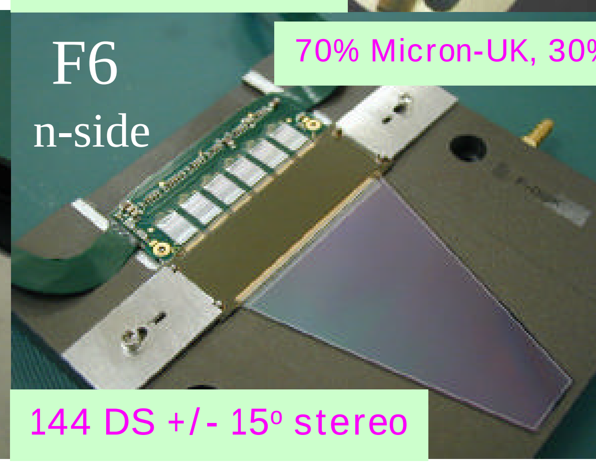


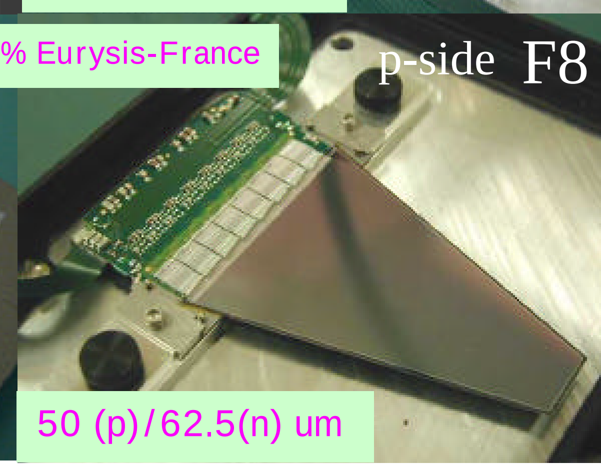
Family of D0SMT Detector types (all AC coupled)



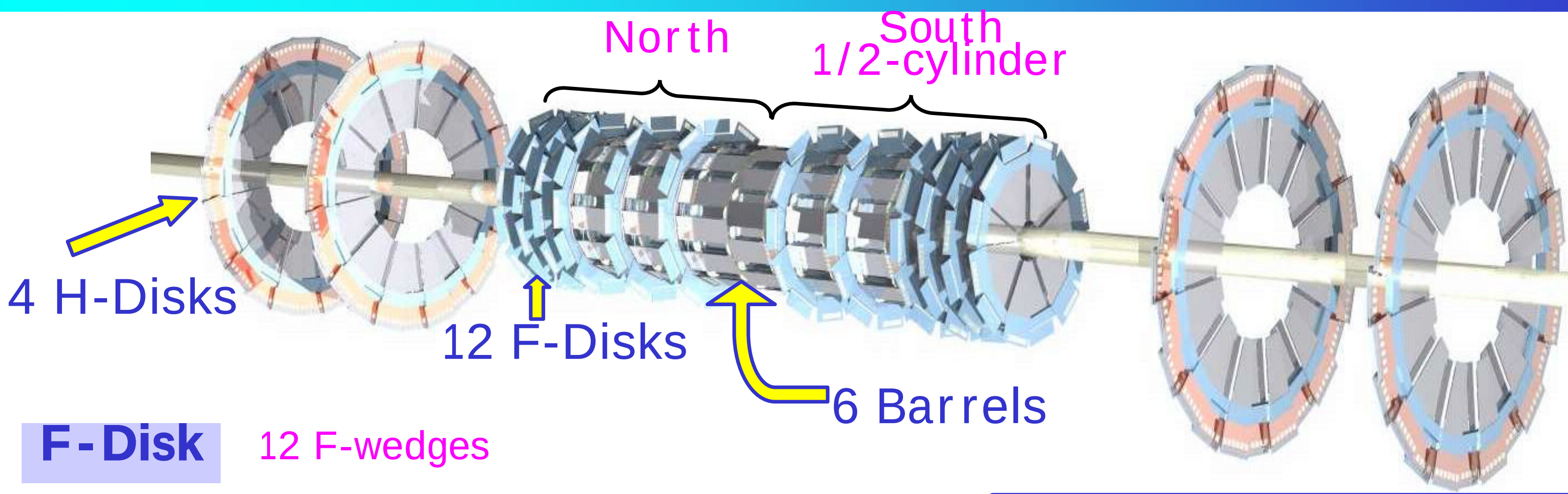








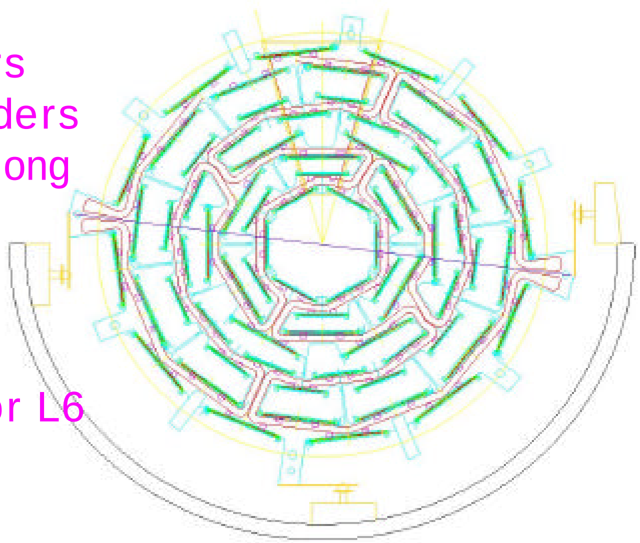
RunIIa SMT Design



F-Disk 12 F-wedges

H-Disk 24 H-wedges

Barrel 8 layers
72 ladders
12 cm long



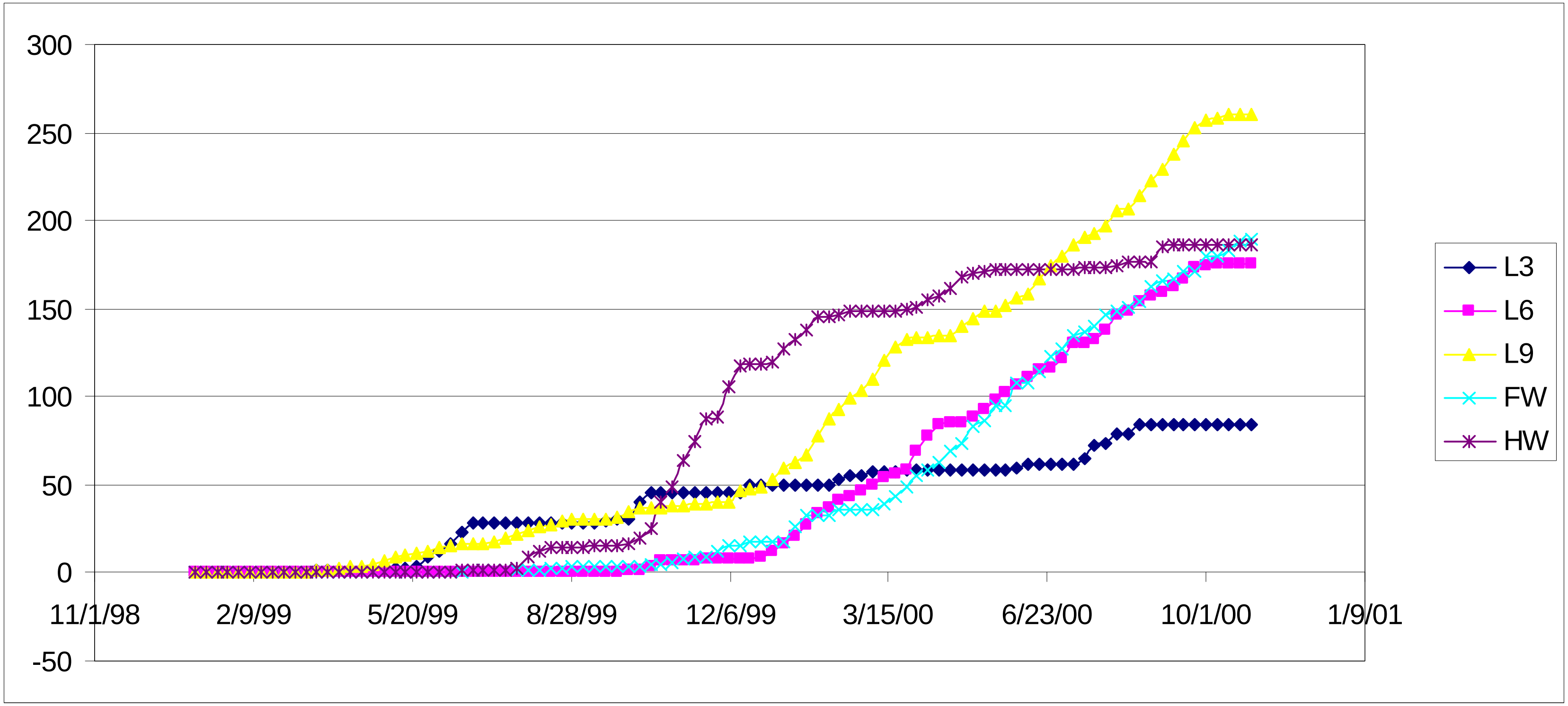
Layers 1,2,5,6: L3 or L6
Layers 3,4,7,8: L9

	Barrels	F-Disks	H-Disks
Channels	387072	258048	147456
Modules	432	144	96
Si Area	1.3 m^2	0.4 m^2	1.3 m^2
Inner R	2.7 cm	2.6 cm	9.5 cm
Outer R	9.4 cm	10.5 cm	26 cm

6192 R/O chips = 792,576 channels
> 1.5 million wire bonds

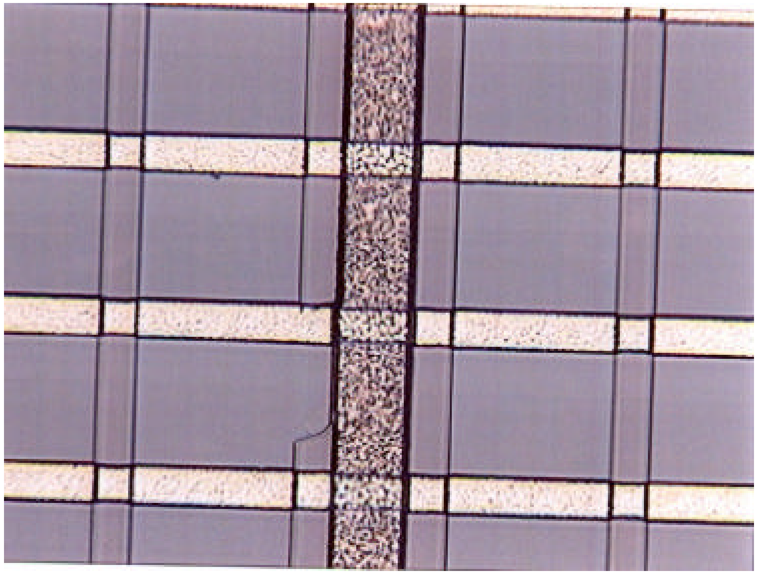
Production: Rates

Production mainly paced by problems with HDIs and Silicon sensors (yields, delivery delays …)



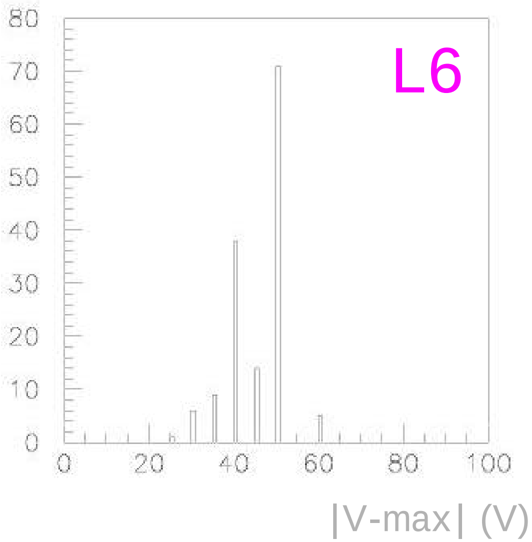
Production: Sensor problems

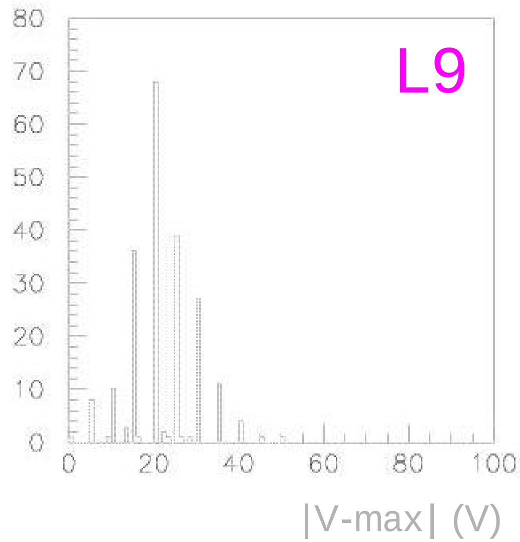
- **Sensor lithography defects**
  - A silicon manufacturing problem produced p-stop isolation defects in the 90° stereo ladders. This resulted in a 30% yield from the manufacturer.

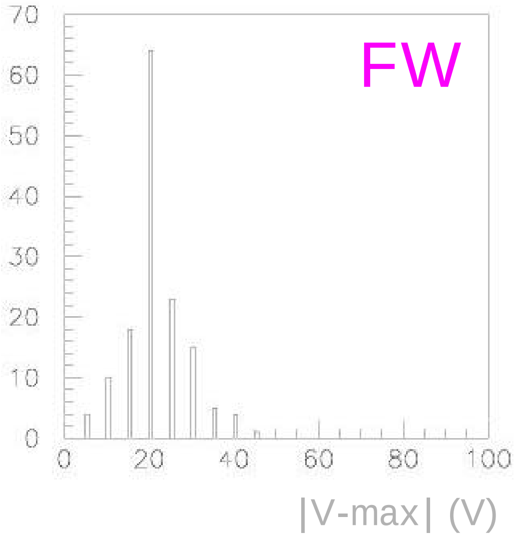


- **Micro-discharge effect**
  - With negative p-side bias on double-sided detectors, we observed micro-discharges producing large leakage currents and noise above a certain breakdown voltage.
  - The effect occurs along the edges of the p implants, where large field distortions and charge accumulations result from misalignment of electrodes with implants.

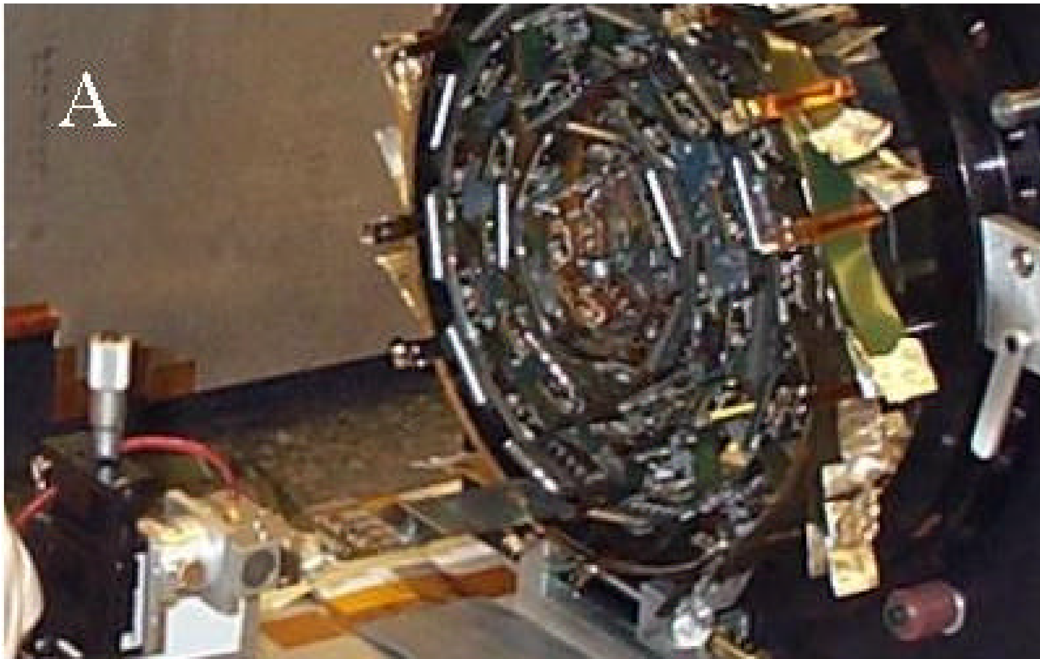
Production: V-max



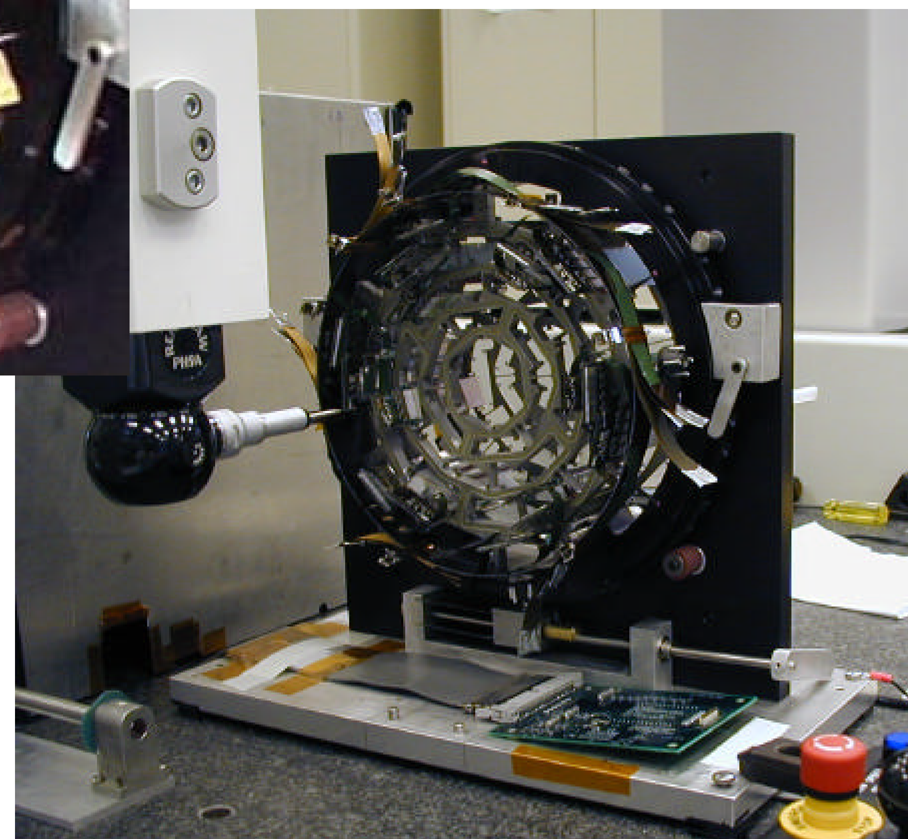




Assembly: Barrel assembly



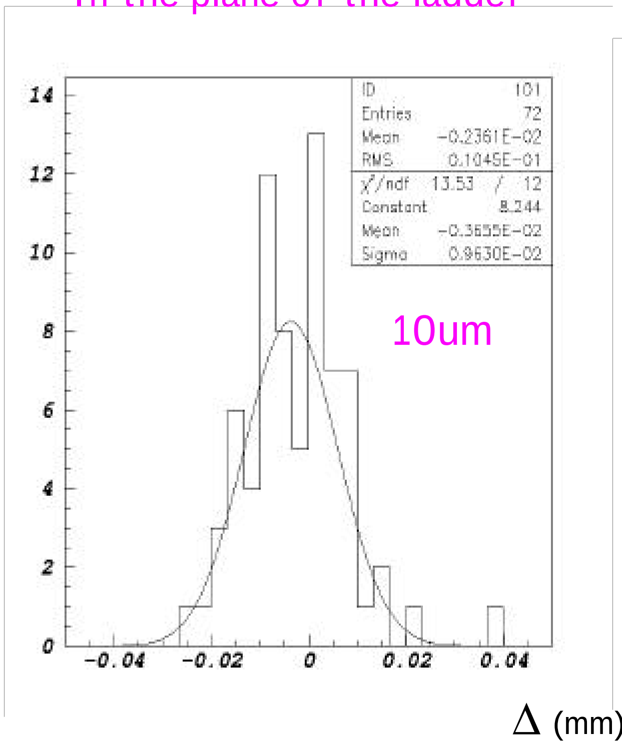
- **Ladders placed on barrels using an insertion fixture**



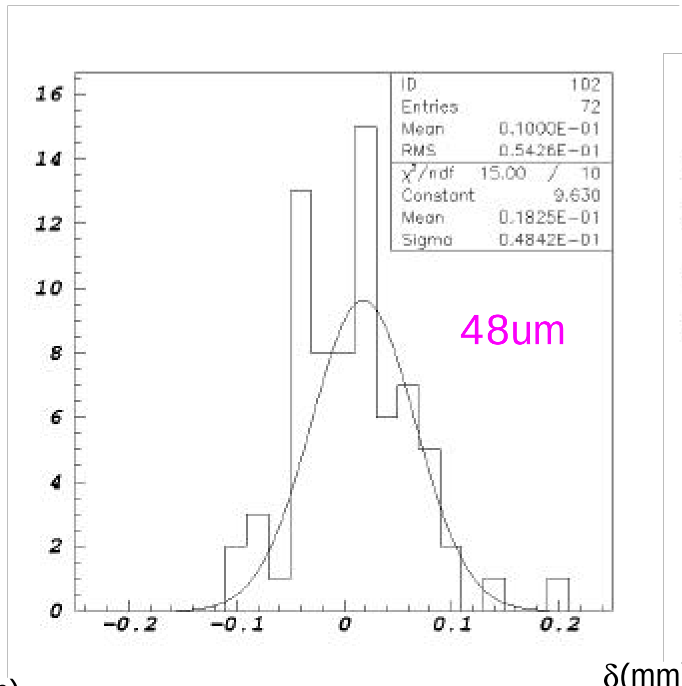
- **Internal alignment done using a CMM (touch probe)**

Assembly: Barrel 2 alignment

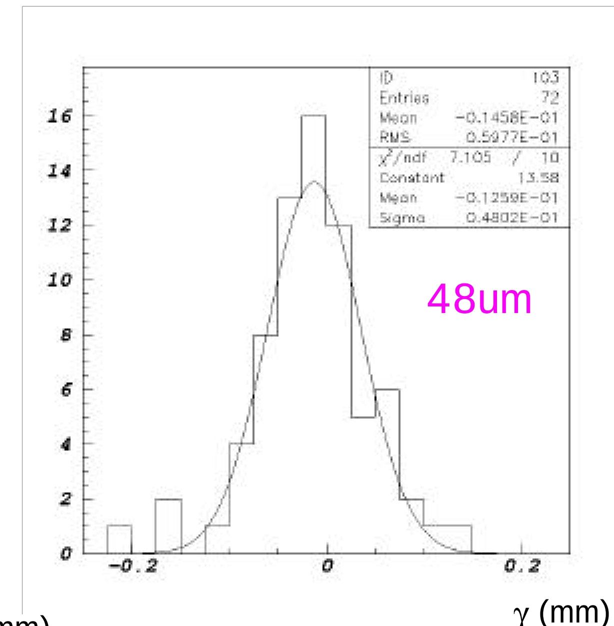
In the plane of the ladder



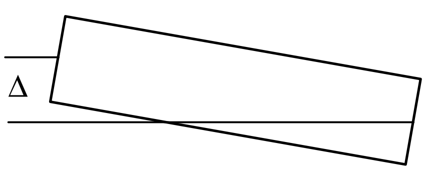
Around ladder short axis



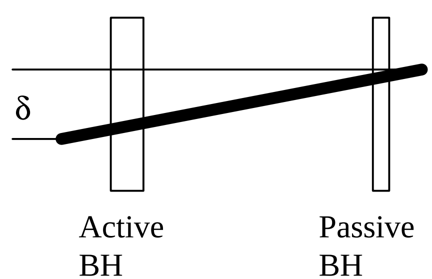
Around ladder long axis



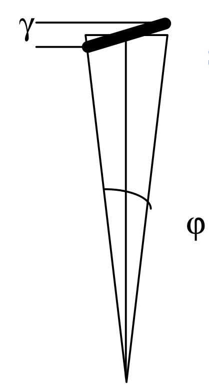
s(D) =10um induces a 3um error



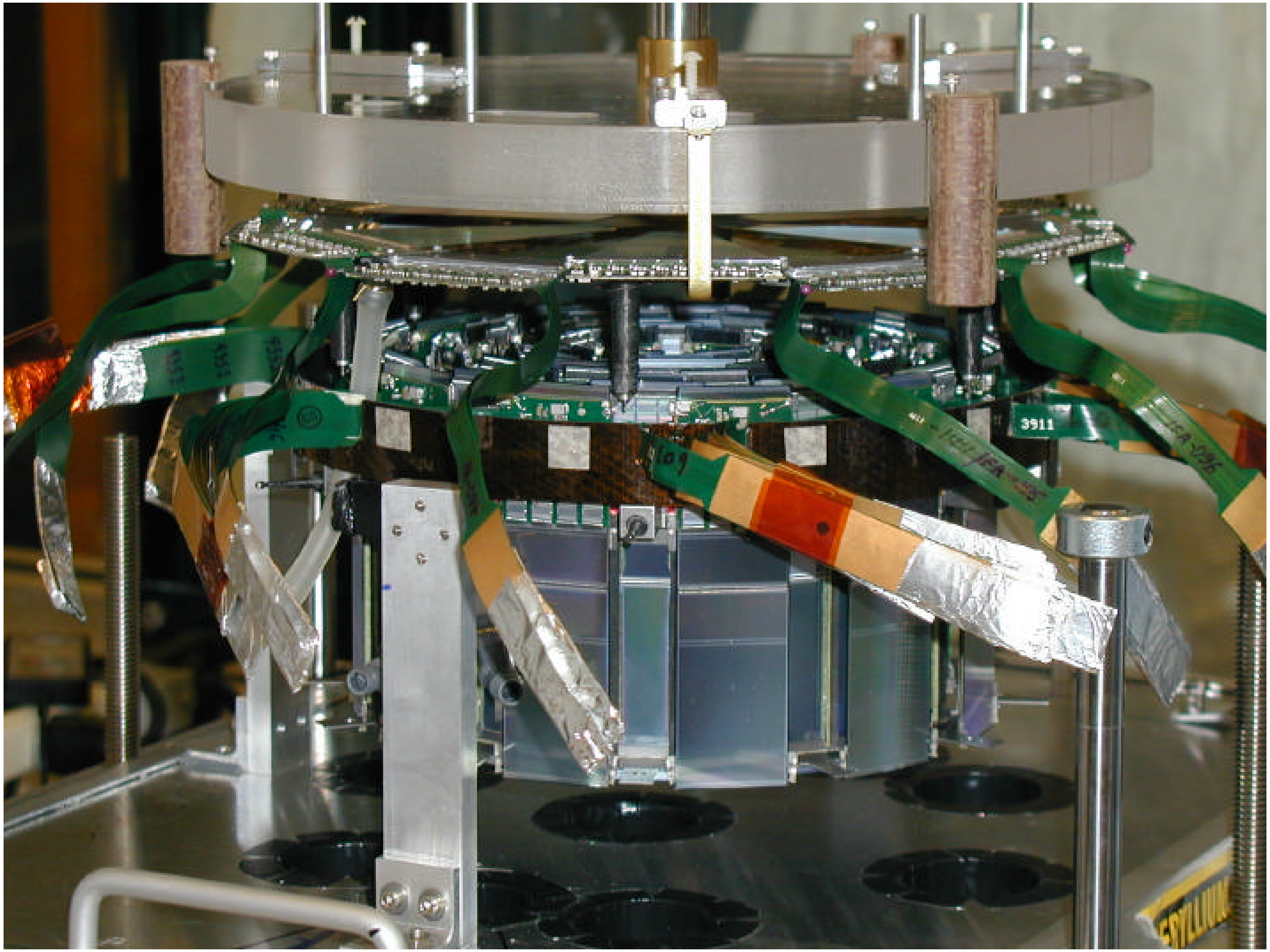
s(d) =48um induces a 3um error



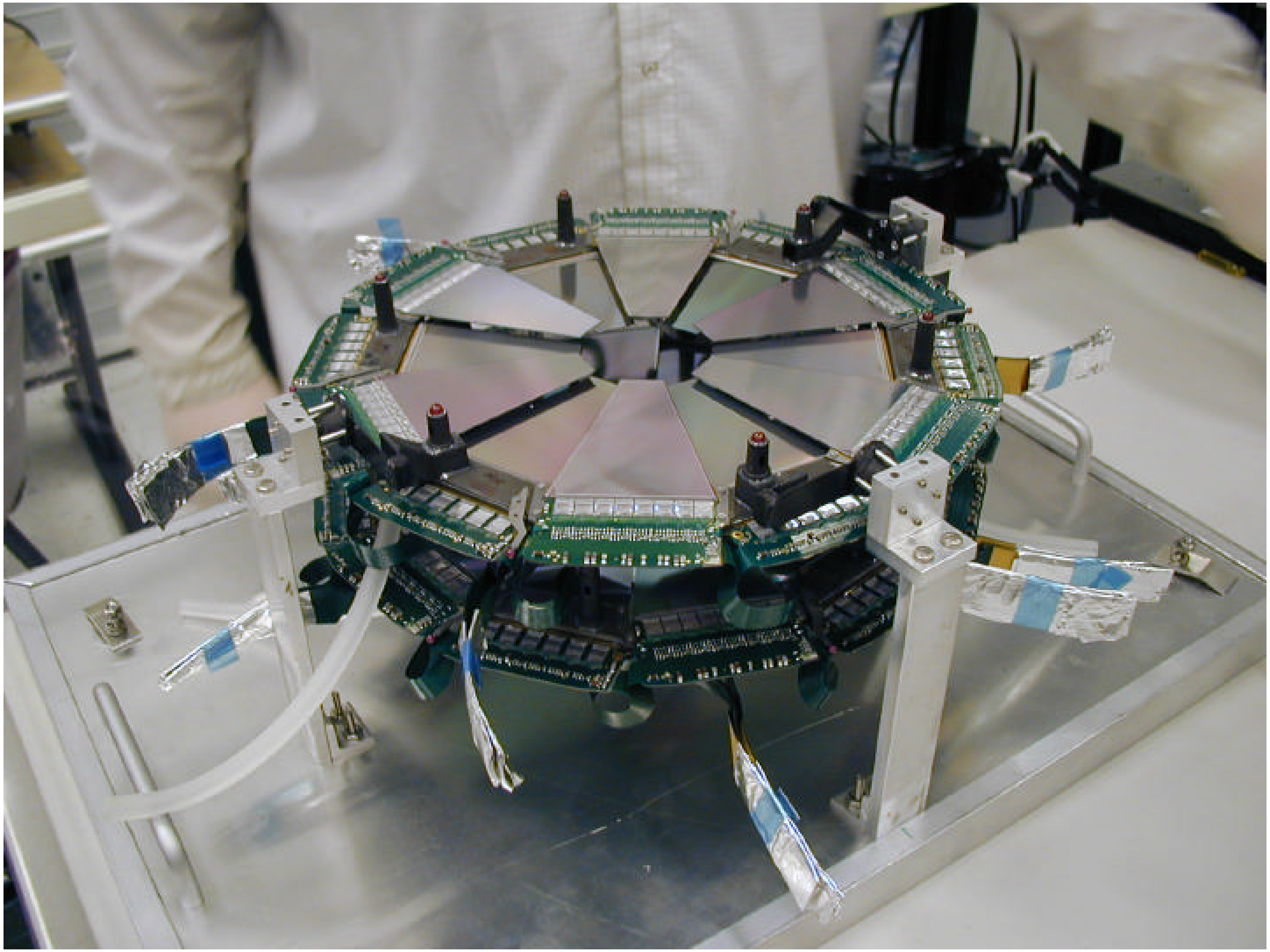
s(g) =48um induces a 2um error



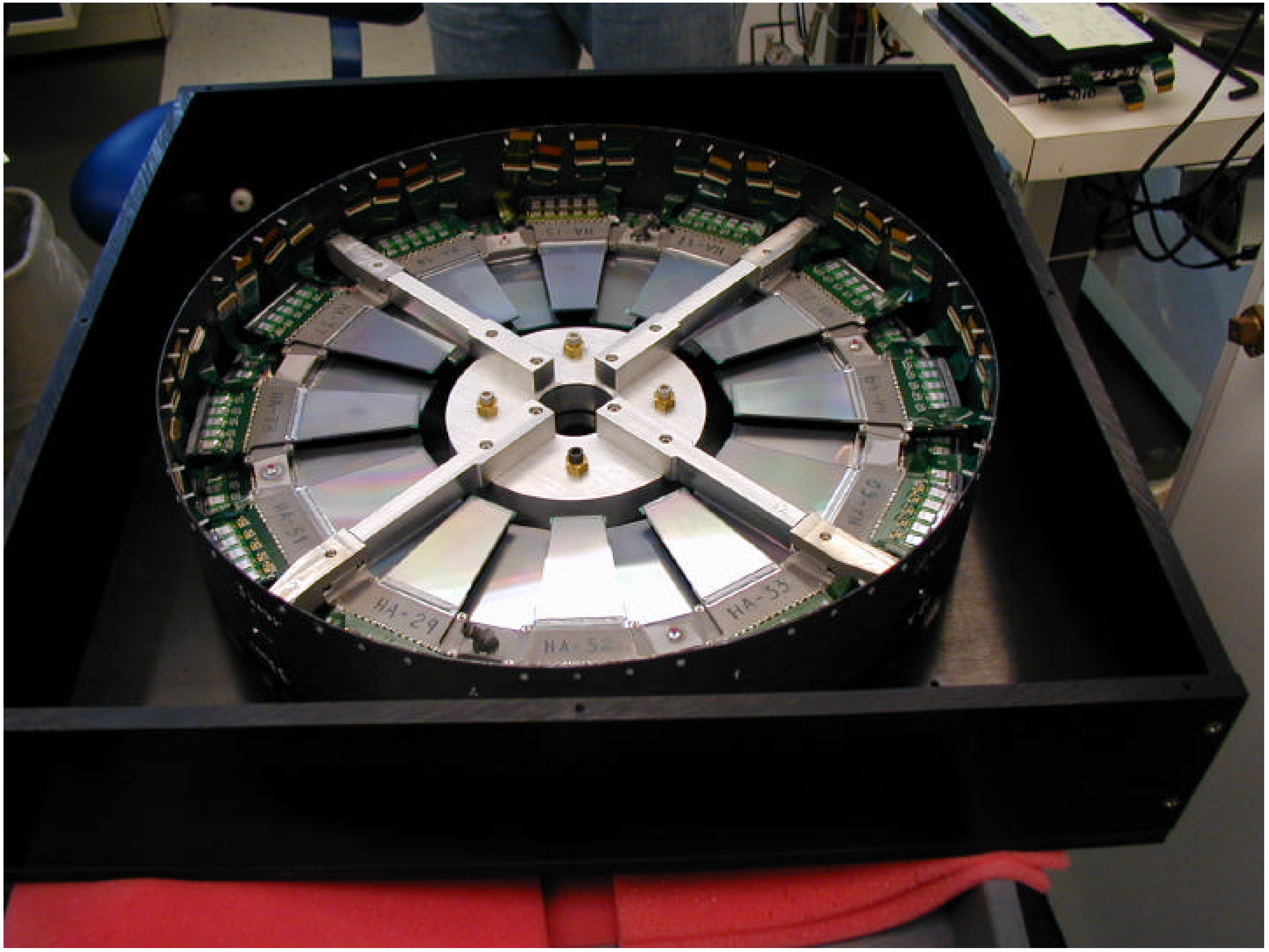
Assembly: Barrel-Fdisk mating



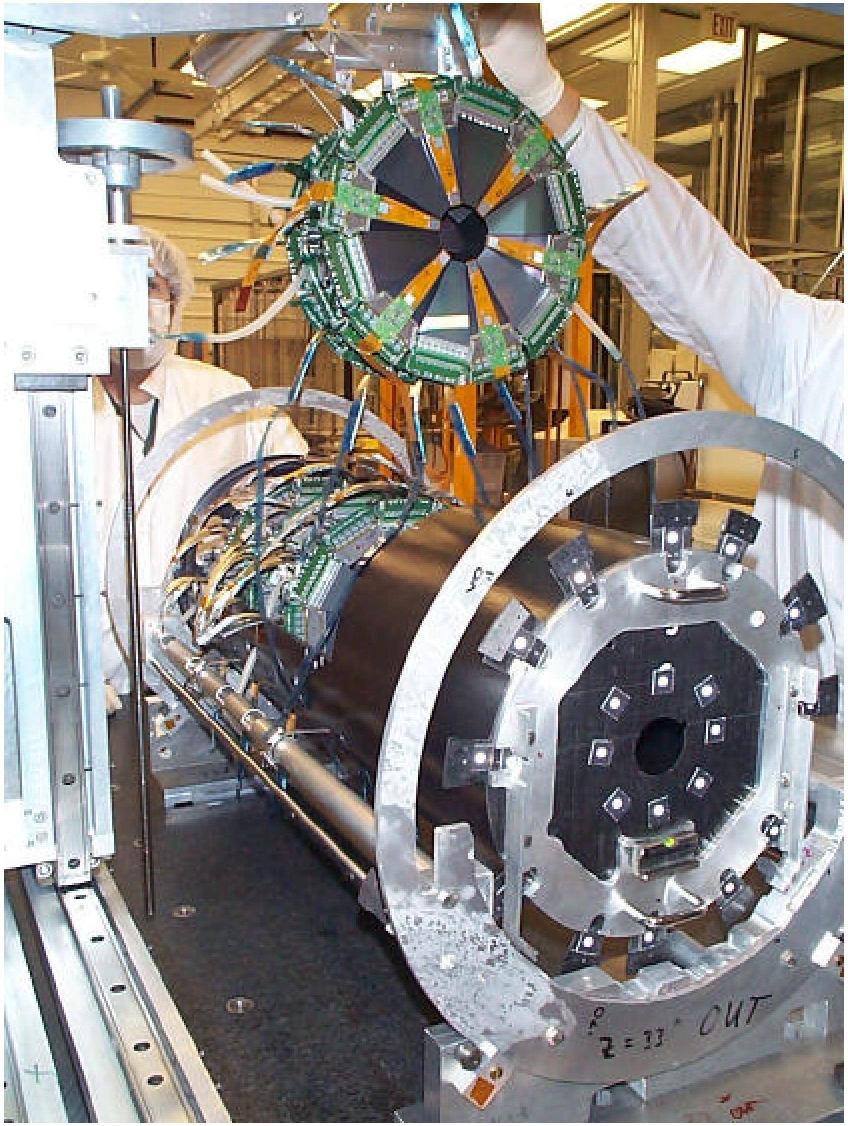
Assembly: End Fdisks mating



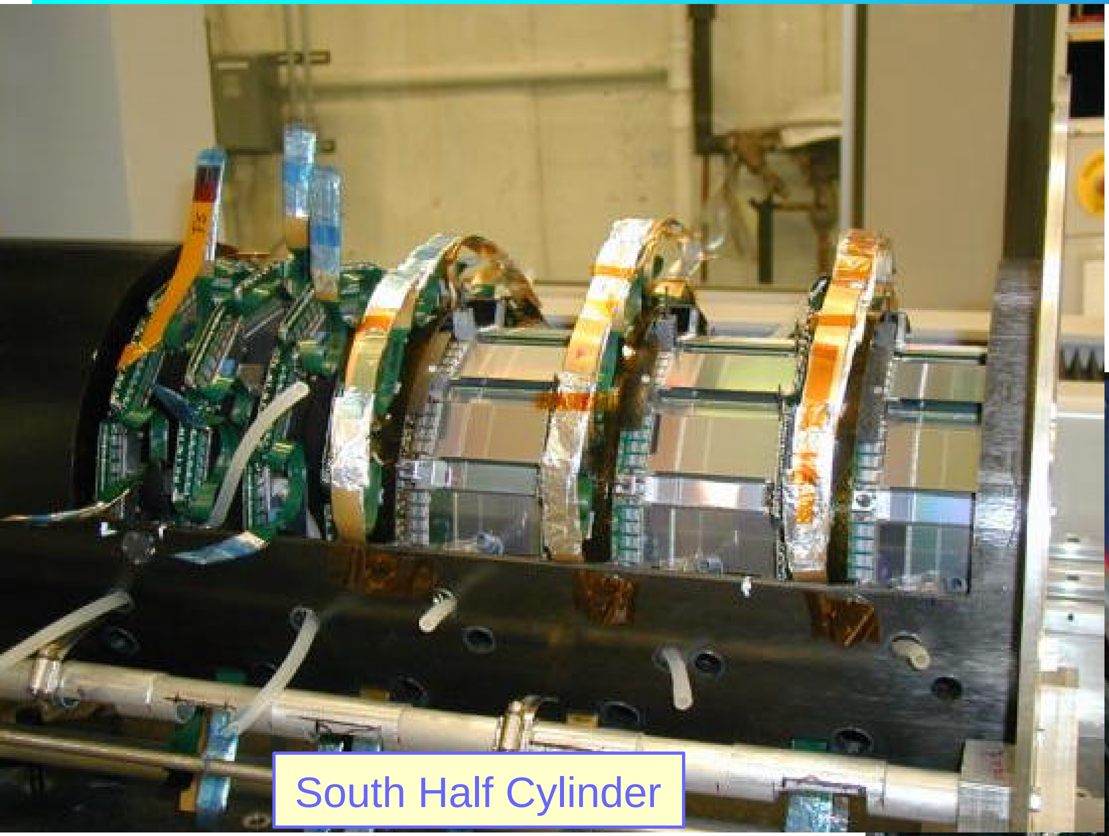
Assembly: Hdisk



Assembly: Radiation monitors

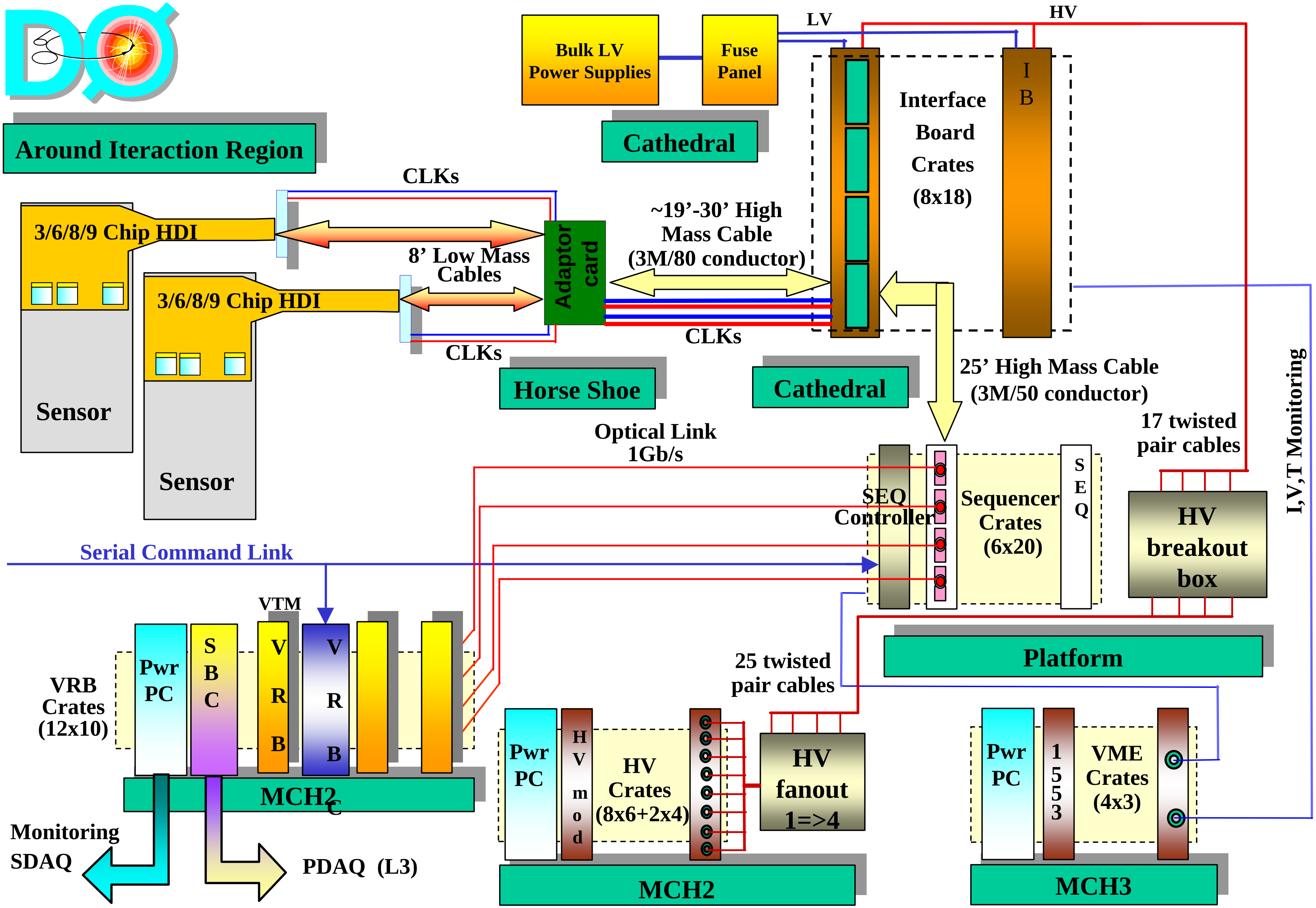


Assembly: 1/2-cylinder



South Half Cylinder

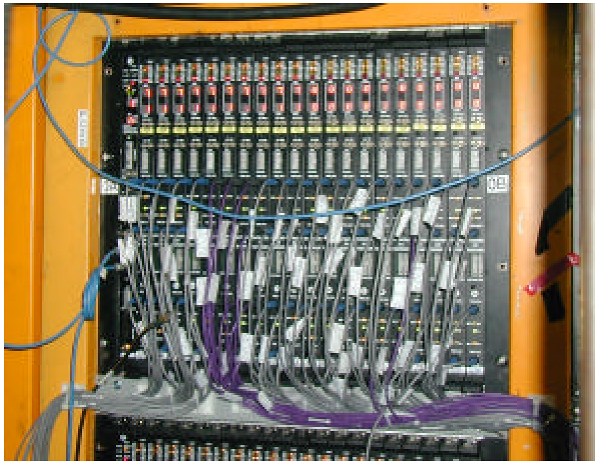
HDI connection to low-mass cable



PowerPCs and Single Board Computers are accessed thru Ethernet

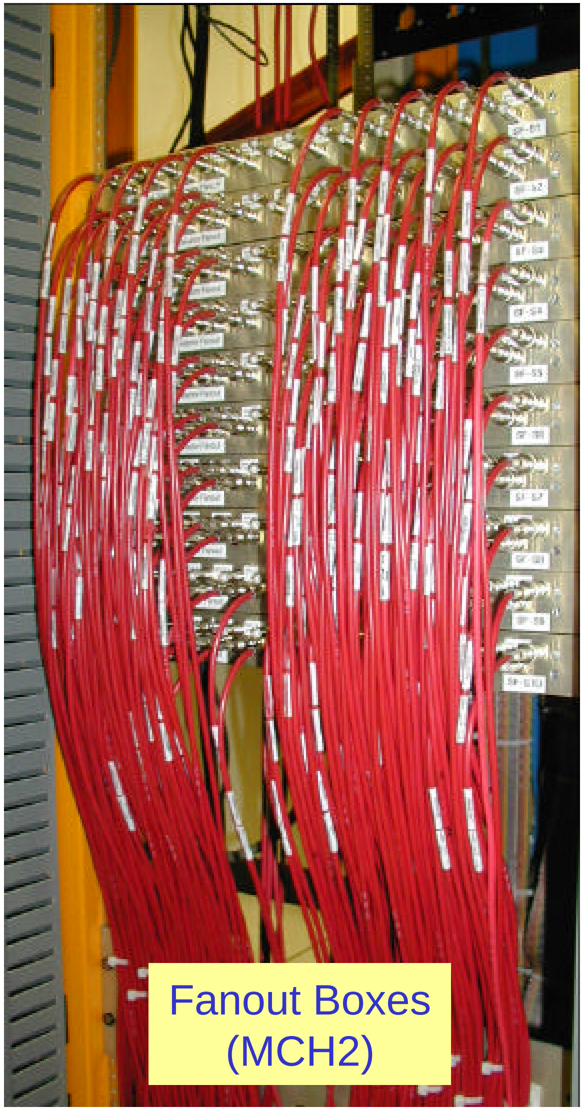
Readout Electronics

- **Interface Boards**
  - 8 crates (144 boards) located inside the detector volume
  - Regenerates signals
  - SVX monitoring and power management
  - Bias voltage distribution
- **SEQuencers**
  - 6 crates (120 boards) located on the detector platform
  - Use SVX control lines to actuate acquisition, digitization and readout
  - Convert SVX data to optical signals
- **VRBs (Readout Buffers)**
  - 12 crates (120 boards) located in counting house
  - Data buffer pending L2 trigger decision
  - Input @ 5-10 kHz L1 accept rate ~ 50 Mb/s/channel
  - Output @ 1 kHz L2 accept rate ~ 50 Mb/s

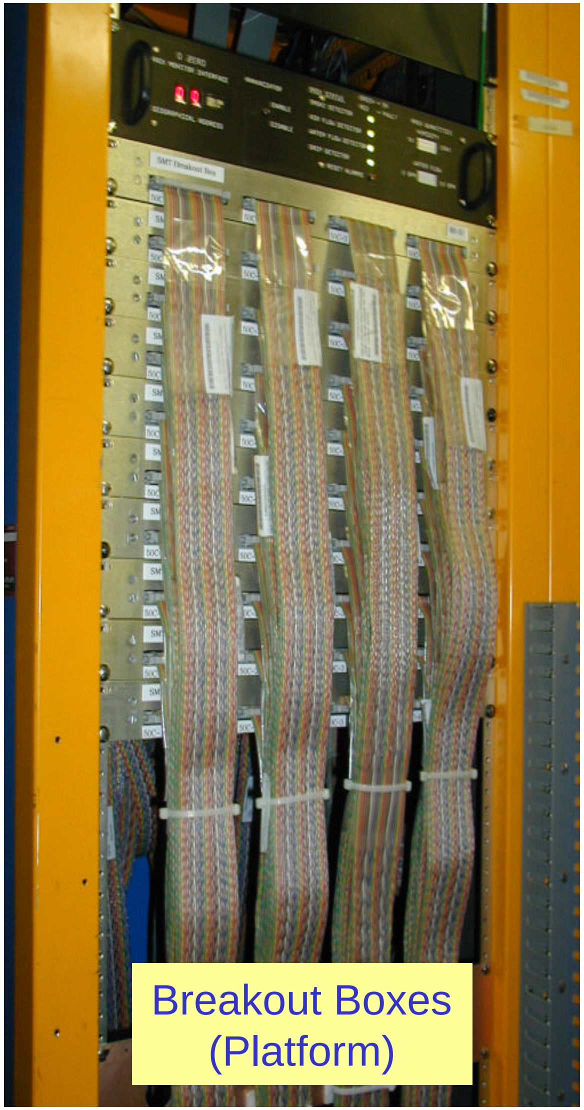


HV distribution

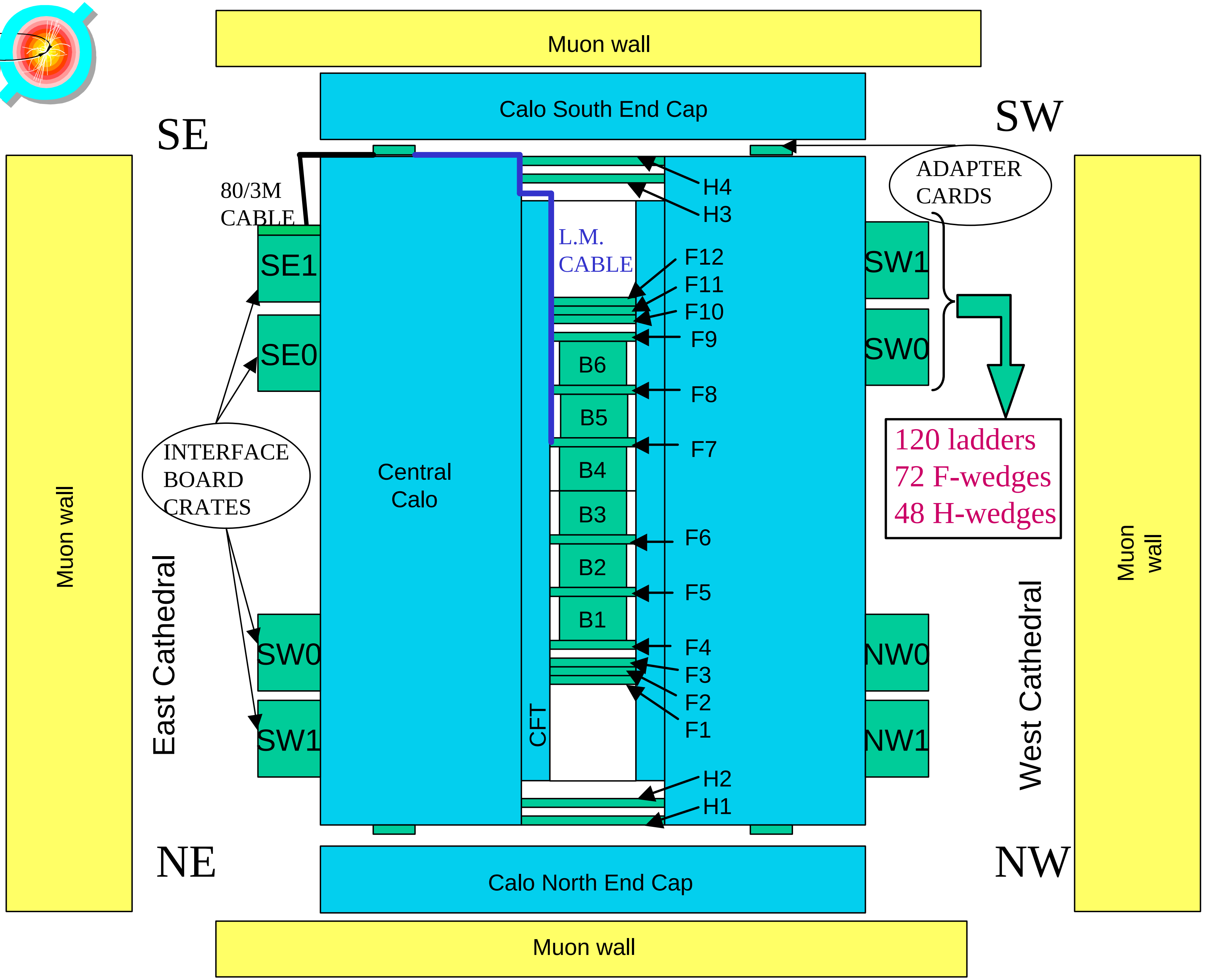
HV Modules
(MCH2)



Fanout Boxes
(MCH2)

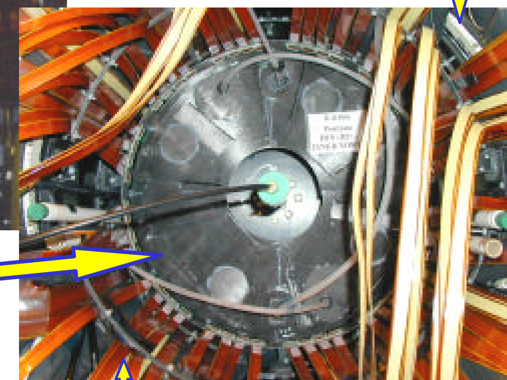


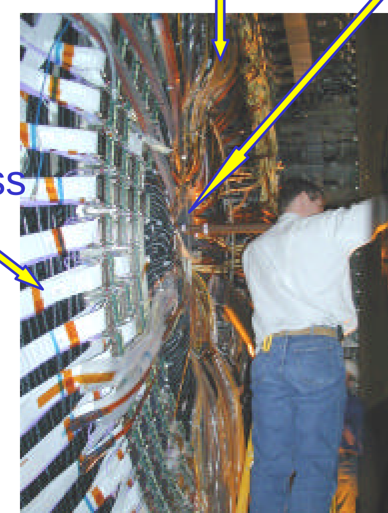
Breakout Boxes
(Platform)


Muon wall
Calo South End Cap
SE
SW
80/3M
CABLE
L.M.
CABLE
H4
H3
ADAPTER
CARDS
SE1
SE0
F12
F11
F10
F9
SW1
SW0
B6
F8
B5
F7
120 ladders
72 F-wedges
48 H-wedges
INTERFACE
BOARD
CRATES
Central
Calo
B4
B3
F6
B2
F5
B1
F4
F3
F2
F1
Muon wall
East Cathedral
SW0
SW1
CFT
NW0
NW1
West Cathedral
Muon
wall
H2
H1
NE
NW
Calo North End Cap
Muon wall

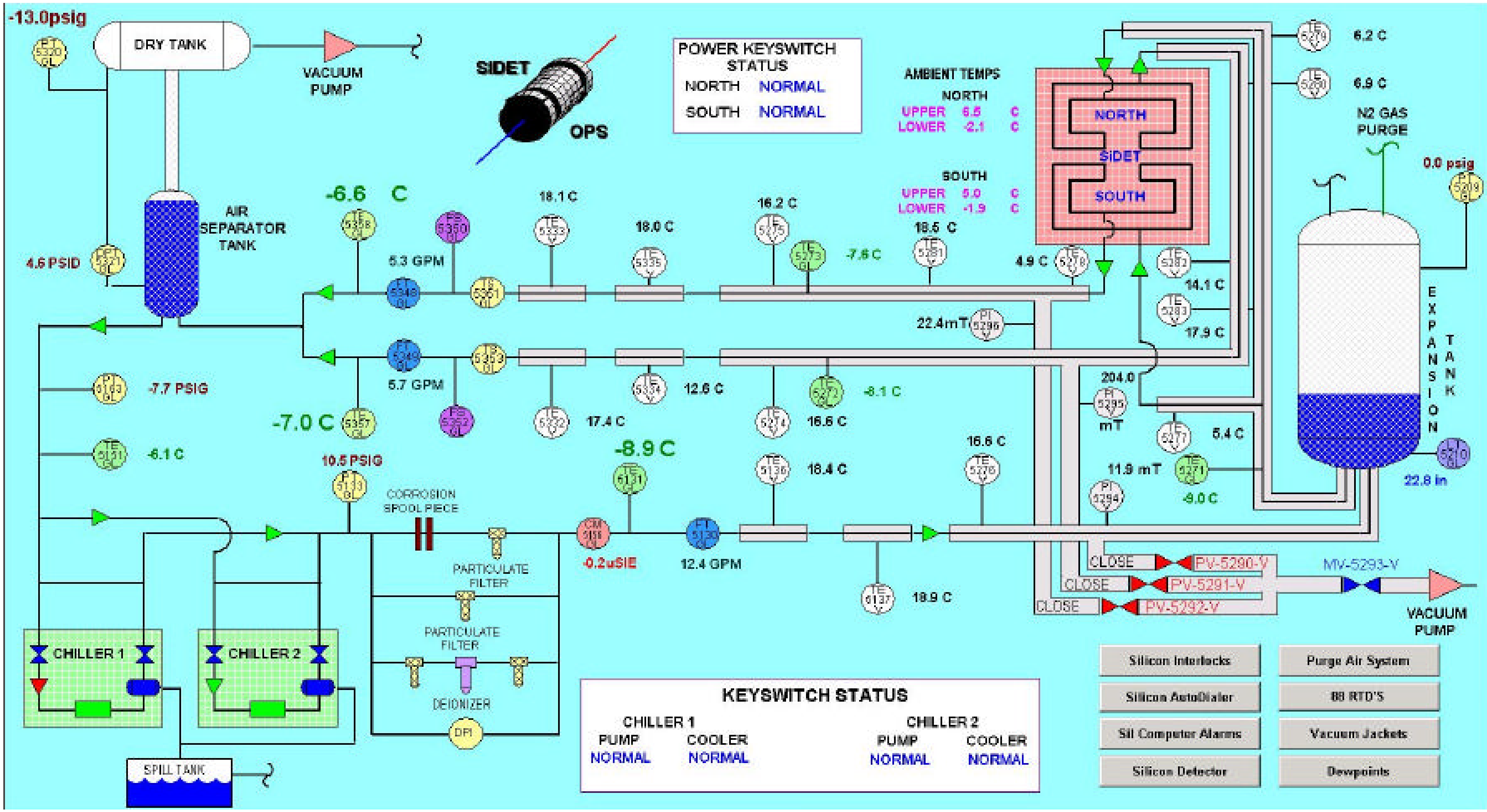
Installation

- **Cylinder installation was completed on 12/20/00**
    - **A 1/2-cylinder of 3 barrels and 6 F disks was inserted into each end of the CFT bore**
- **H Disk installation was completed on 2/6/01**
- **The cabling (~15,000 connections) and electronics installation was completed in May 2001**





Installation: Cooling system



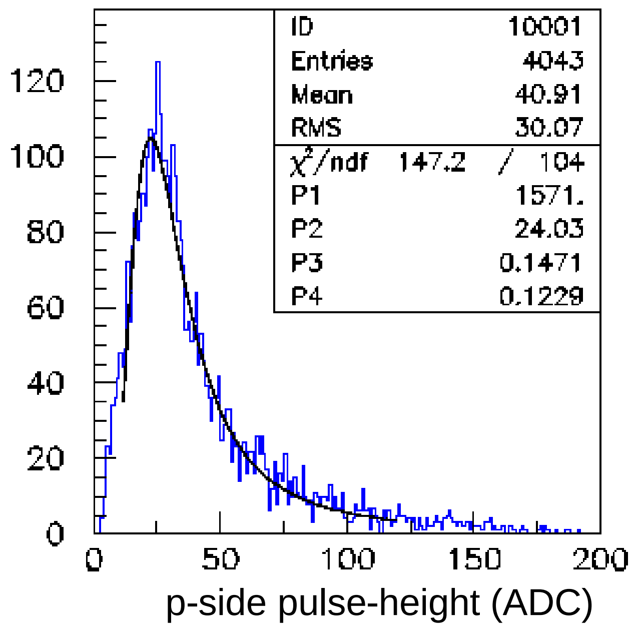
- 30% glycol + water at –10 ºC (=> detectors between –5 and 0 ºC)
- The tracking volume is purged with dry air to prevent condensation

Commissioning: Status

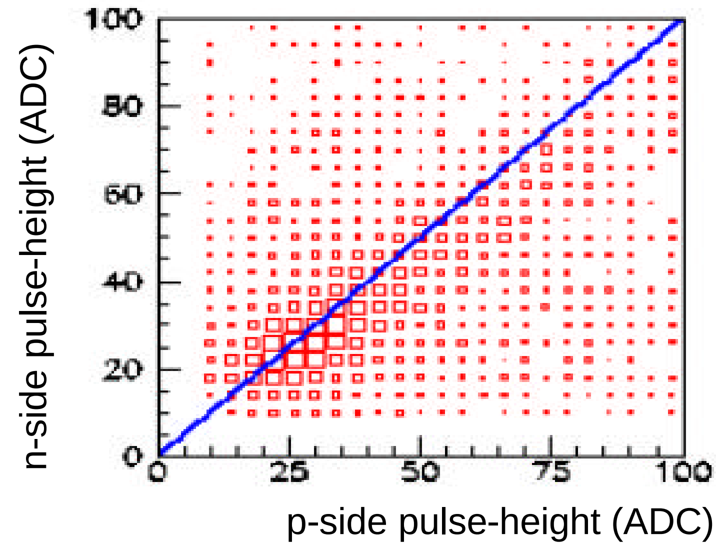
- entire detector is connected and powered
- currently collecting essentially physics data. Calibration and commissioning data when no beam present
- some problems we run into:
  - had failure of some IB LV PS. Fixed and reliable now.
  - IB crate heat exchangers water leak
    => had to disconnect 2 out of 8
  - Hygroscopicity and not-too-professional assembly of some HV fan out boxes leading to bias current instabilities => tried to fix them but designed and ordered new ones
  - Failure of a few detectors since the last shutdown
    => not necessarily an HDI problem. Part of them will be fixed in January 2003. Fraction of enabled detectors:
    - on 12/01/01: 93% (Barrels) - 95% (F-Disks) - 90% (H-Disks)
    - on 09/31/02: 89% (Barrels) - 94% (F-Disks) - 84% (H-Disks)

Commissioning: Charge collection

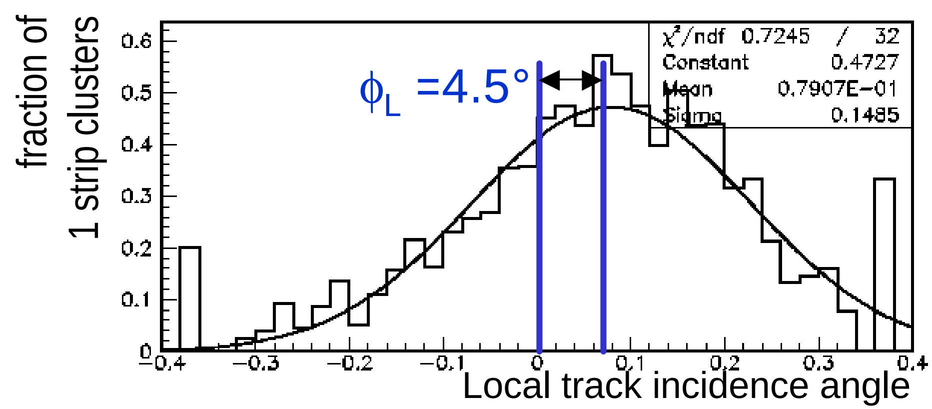
- Cluster charge (corrected for track angle): 1 mip ~ 25 ADC counts. Noise < 2ADC counts.



- Charge correlation between p- and n-side of a detector

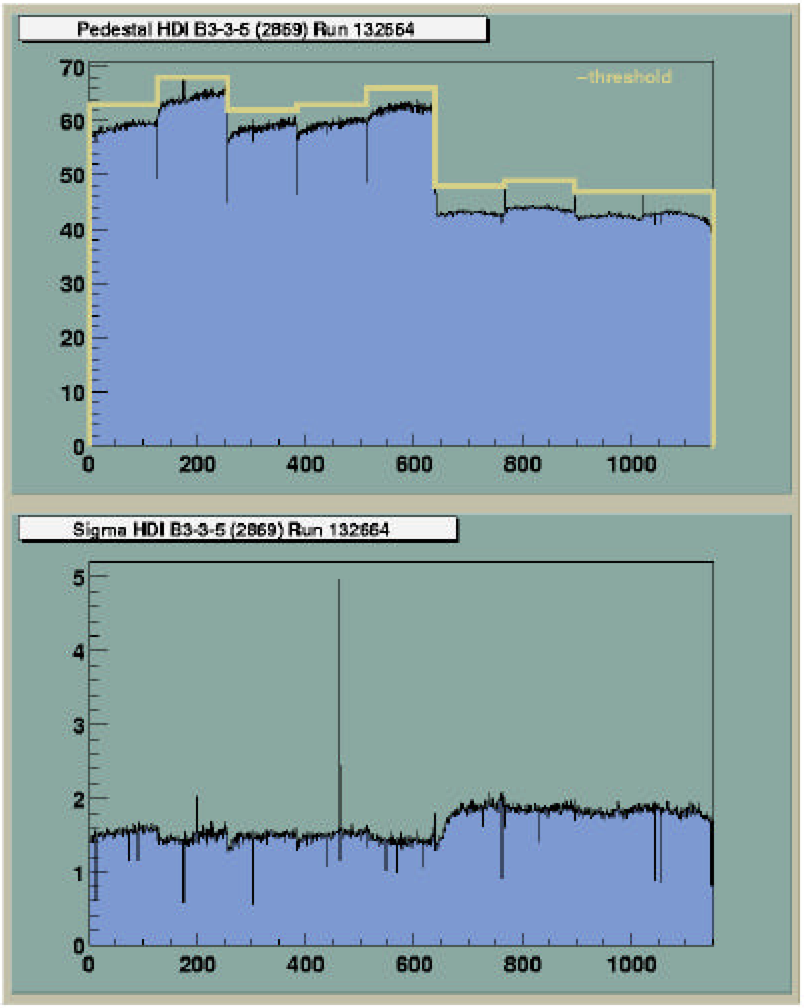


- Lorentz angle: The charge deflection due to the magnetic field

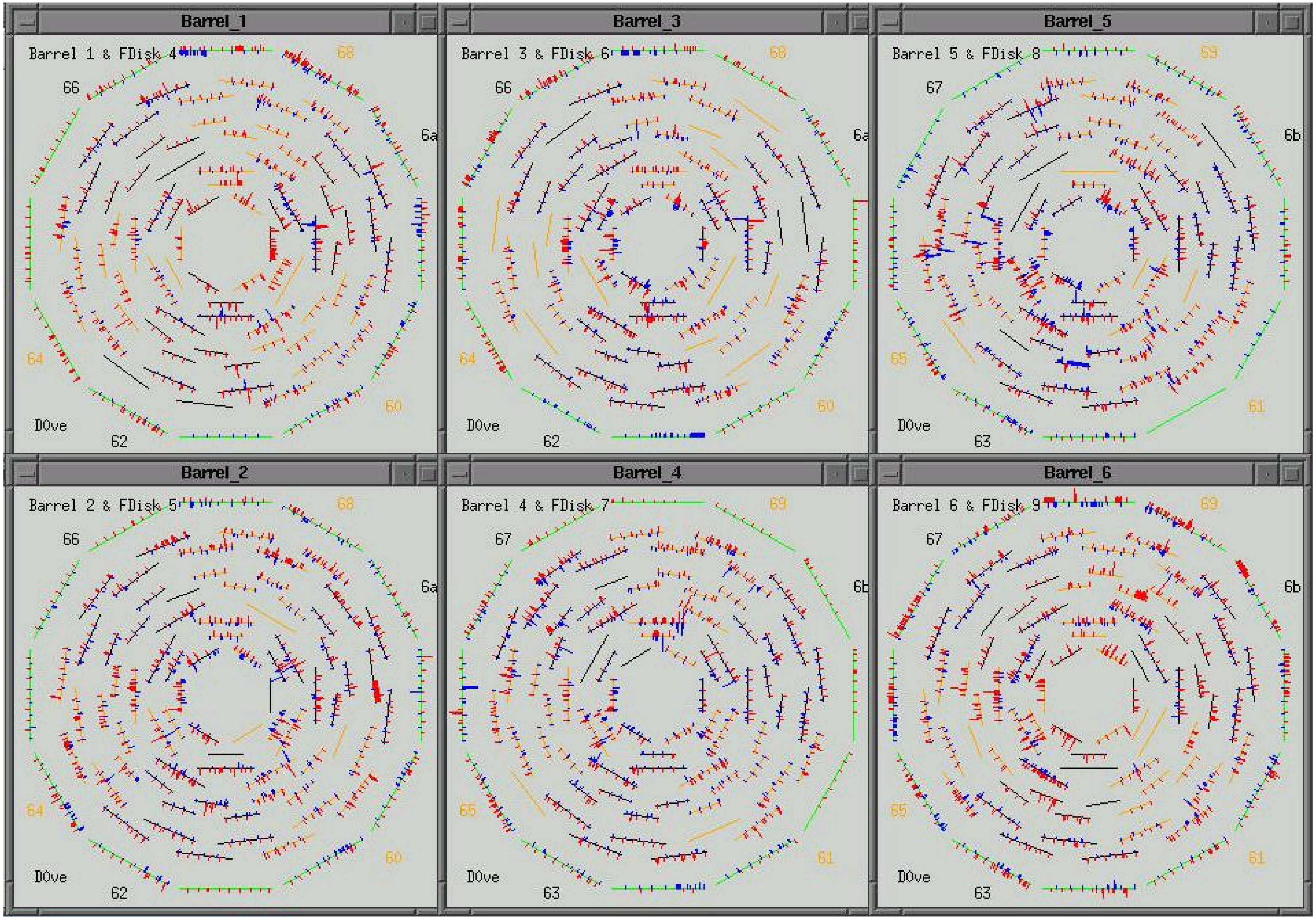


Operations: Calibrations

- SMT pedestal, noise and gain measurements are taken using SDAQ.
- Pedestal and noise measurements are used to calculate the threshold per chip to be used in sparse read out

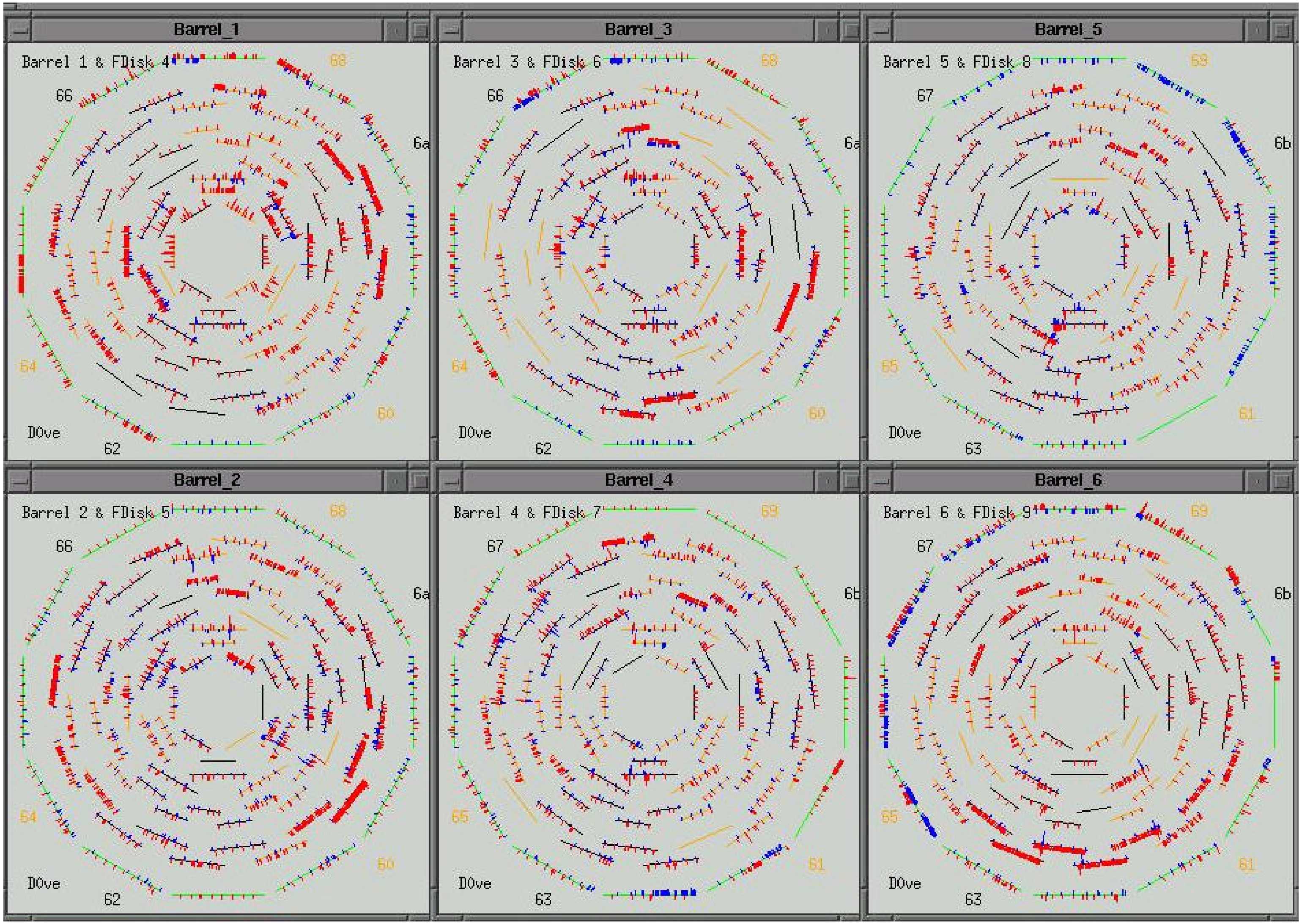


Operations issues



a quiet event

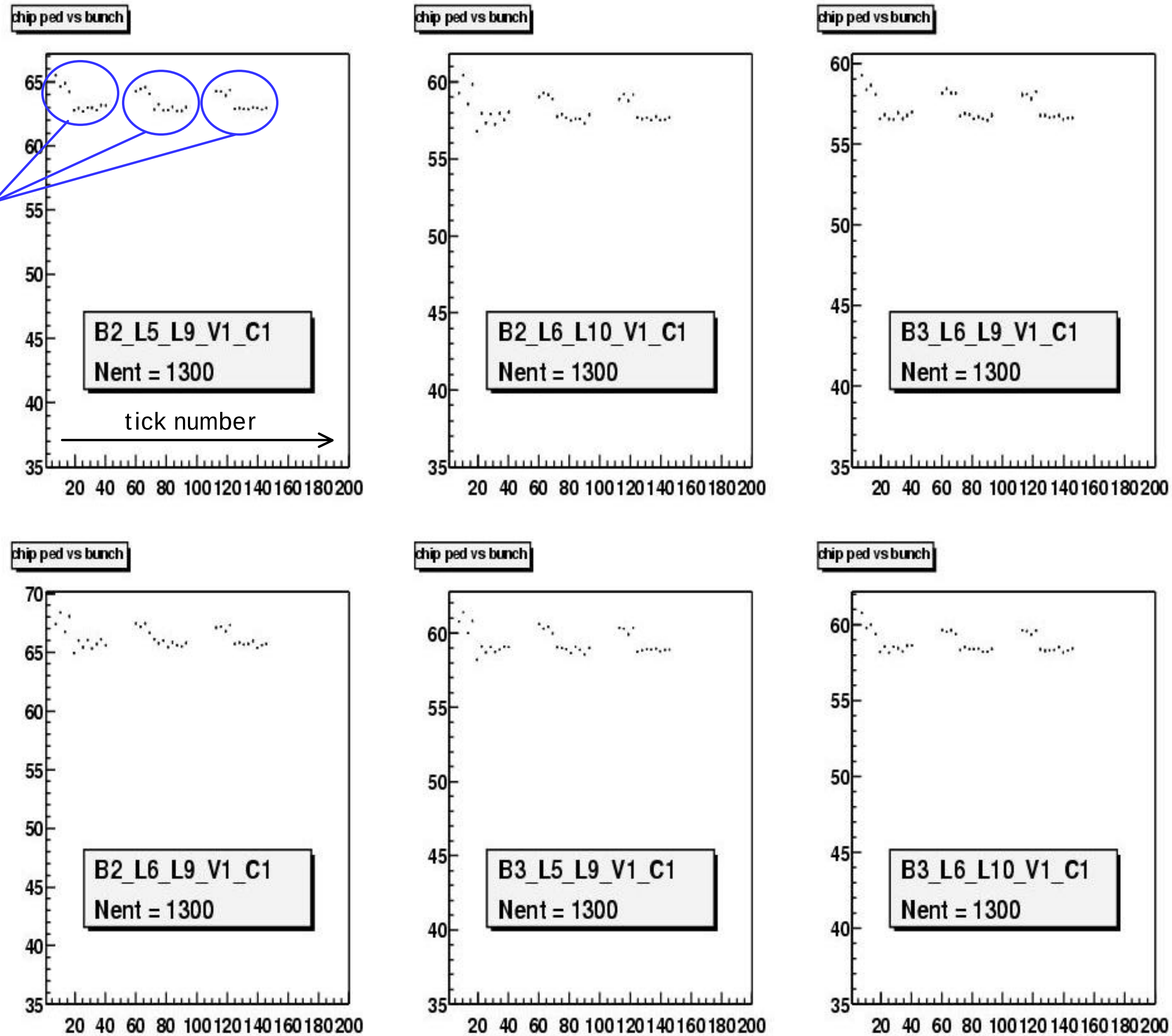
Operations issues



a busy event

Operations issues: Pedestal shifts

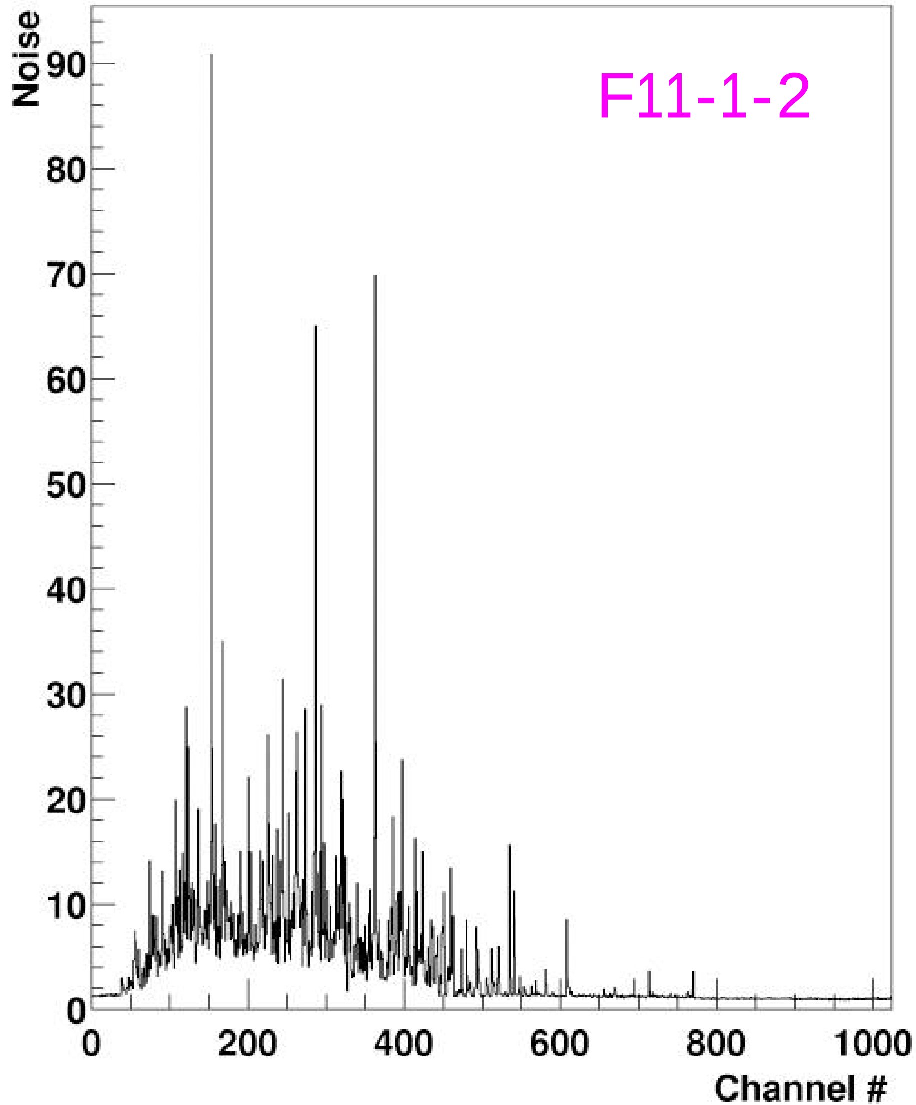
3 superbunches of 12 bunches



- **pedestals seem to be different at the beginning of each superbunch**
- **Investigating ...**

Operations issues: F-Wedges noise (1)

- seems to affect only the p-side of a fraction of the Micron sensors
- does not seem to depend on the biasing scheme
- does not seem to depend on temperature
- still investigating ...

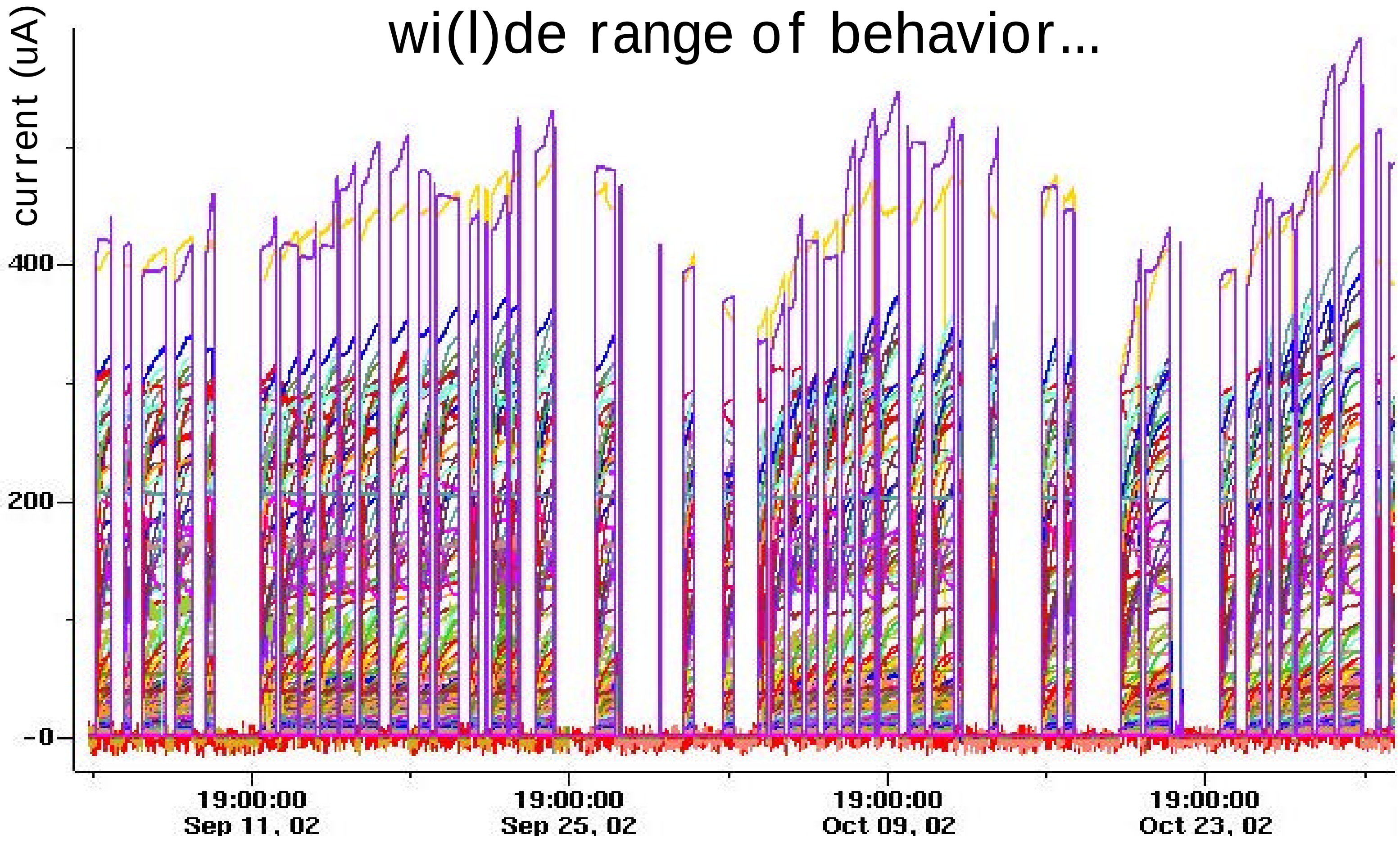


Operation issues: F-Wedges noise (2)

# of wedges in disk	w/ > 10% noisy strips				w/ > 20% noisy strips				w/ > 30% noisy strips			
	P-side			N-side	P-side			N-side	P-side			N-side
threshold (ADC)	4	6	10	4	4	6	10	4	4	6	10	4
01 (Micron)	6	4	1	3	2	2	1	1	1	1	0	0
02 (Micron)	4	1	0	1	2	0	0	1	1	0	0	1
03 (Eurysis)	0	0	0	0	0	0	0	0	0	0	0	0
04 (Micron)	5	4	2	2	4	3	1	1	3	2	1	1
05 (Eurysis)	0	0	0	1	0	0	0	1	0	0	0	0
06 (Micron)	7	5	5	7	6	5	3	4	4	3	2	4
07 (Micron)	3	2	2	1	2	2	1	0	1	1	0	0
08 (Eurysis)	0	0	0	0	0	0	0	0	0	0	0	0
09 (Micron)	4	4	3	2	4	3	1	1	2	2	0	1
10 (Eurysis)	0	0	0	0	0	0	0	0	0	0	0	0
11 (Micron)	5	3	3	4	3	2	0	1	2	1	0	0
12 (Micron)	6	3	2	2	2	2	2	0	2	2	0	0
TOTAL (144)	40	26	18	23	25	19	9	10	16	12	3	7

Bias currents: first look (1)

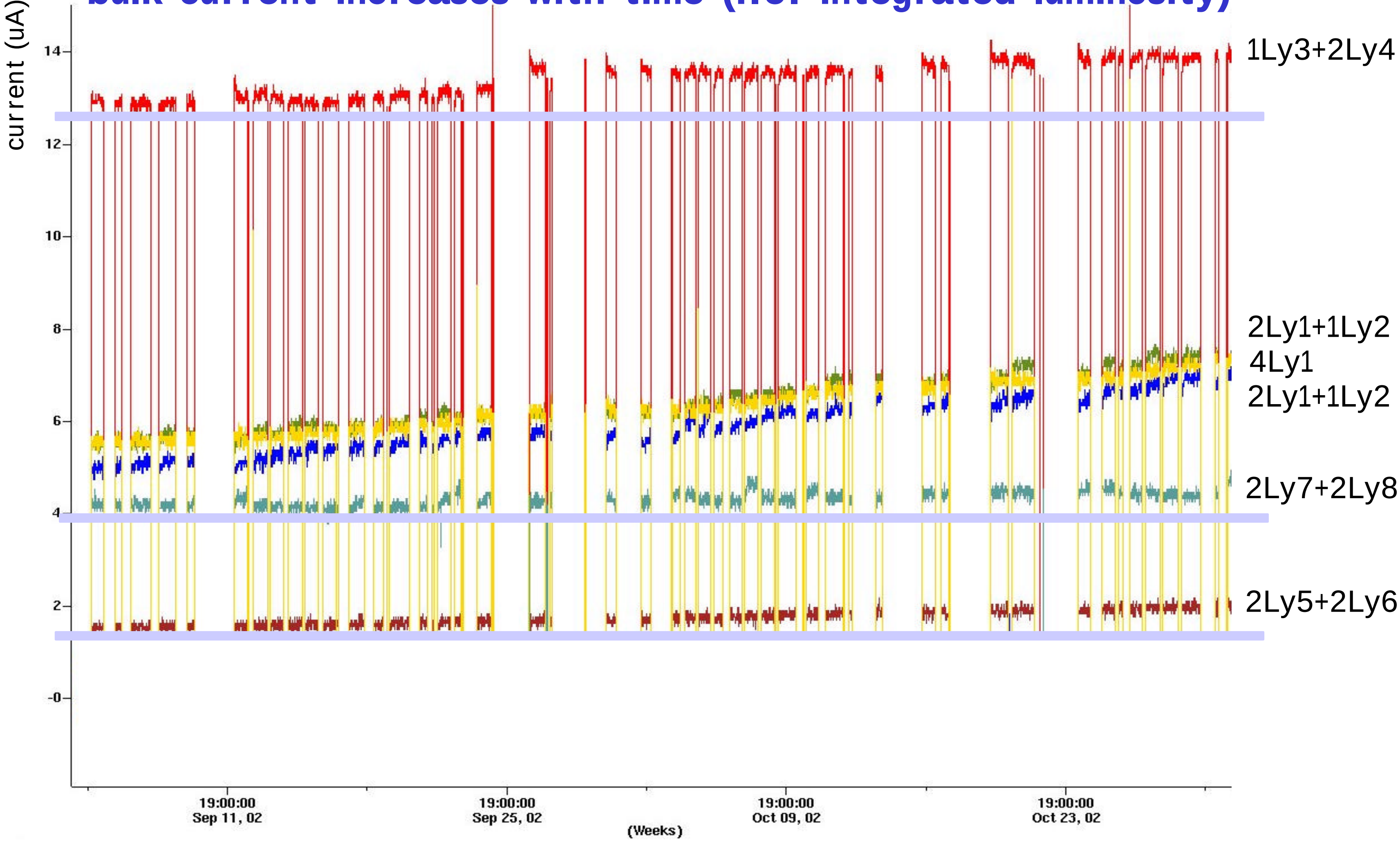
wi(l)de range of behavior...



this is not bulk current.

Bias currents: first look (2)

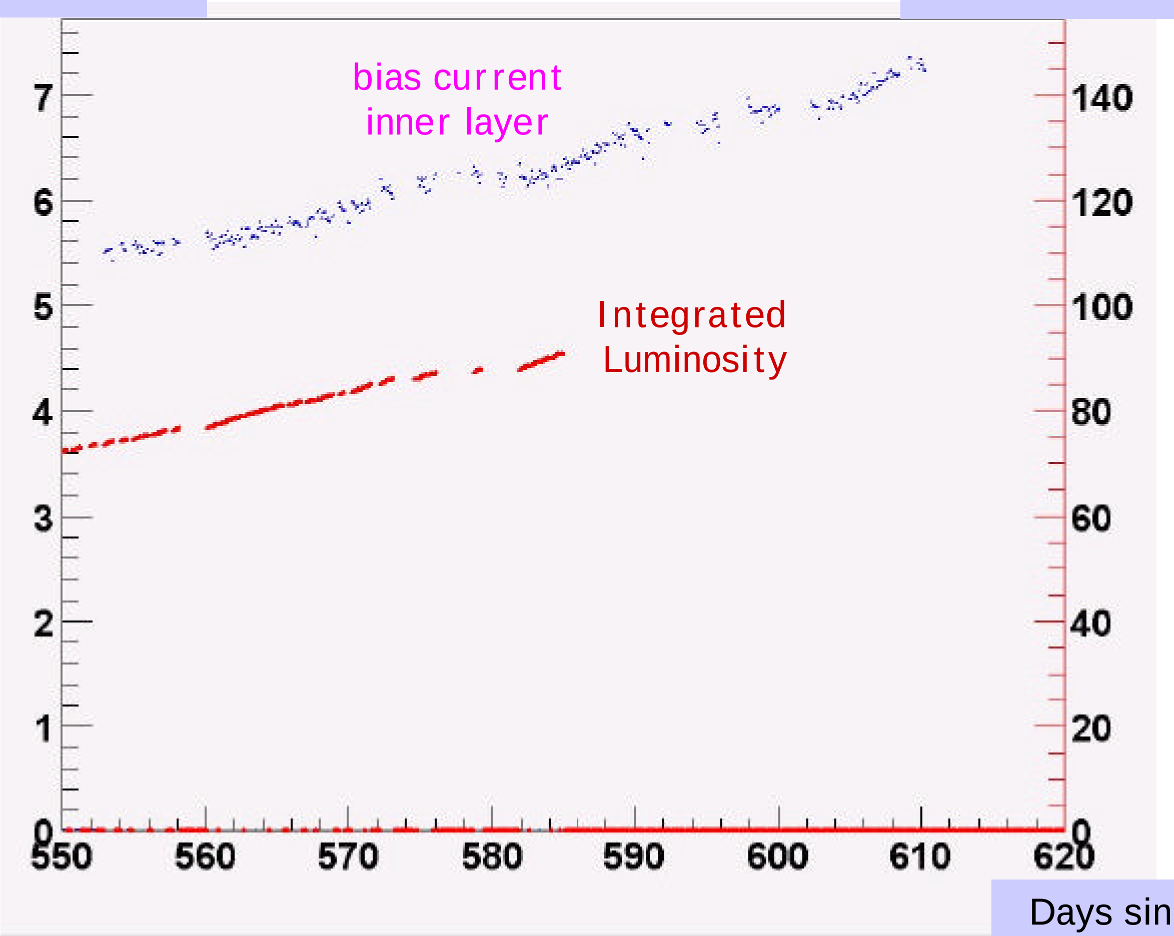
- As expected, the closer you get from the beam and the fastest the bulk current increases with time (i.e. integrated luminosity)



Bias currents: first look (3)

current (uA)

Integrated Luminosity (pb-1)



Days since 03/01/2001

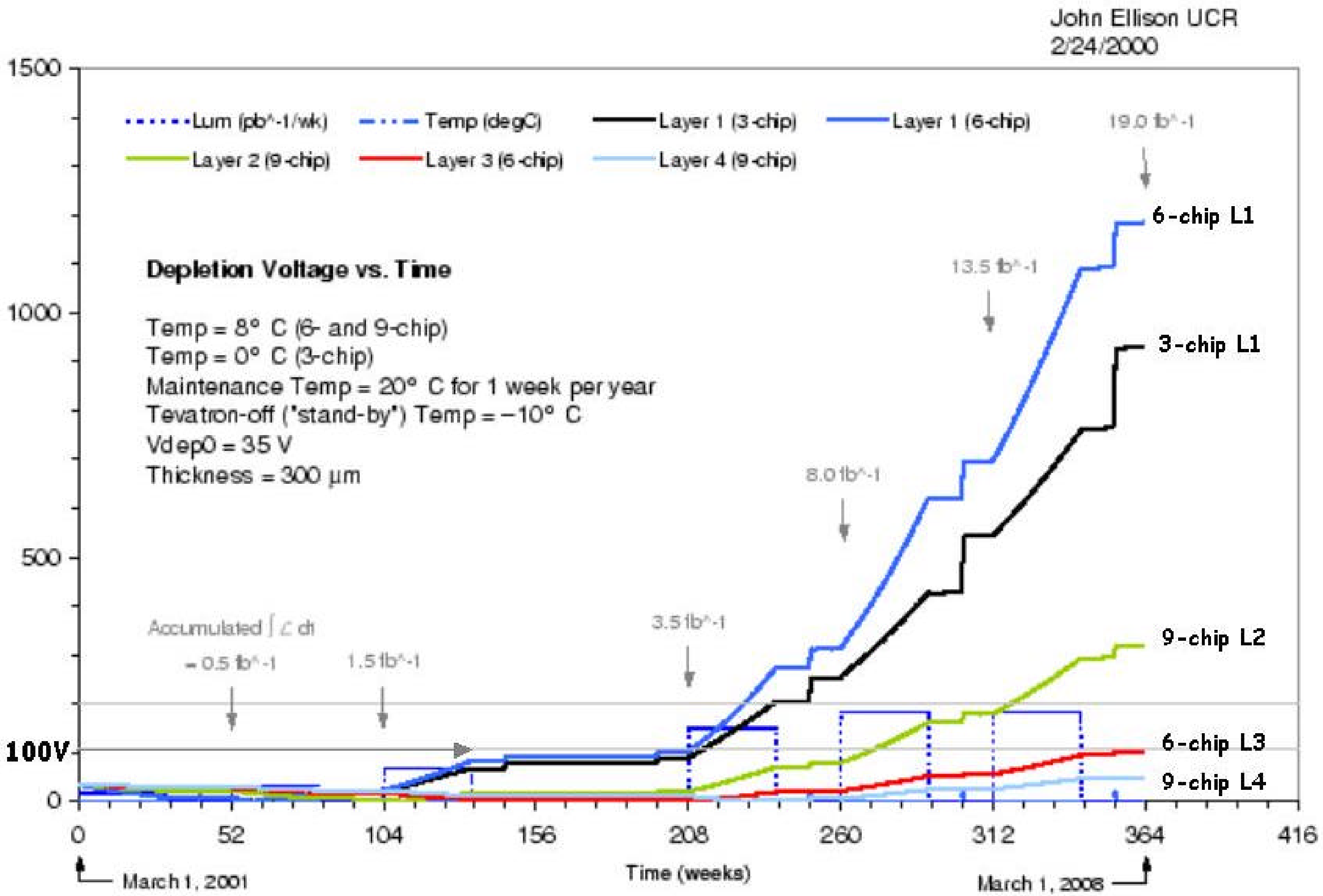
Roughly scales with luminosity

back of the envelop calculation:

1uA/20pb^{-1} => 100uA/2fb^{-1}

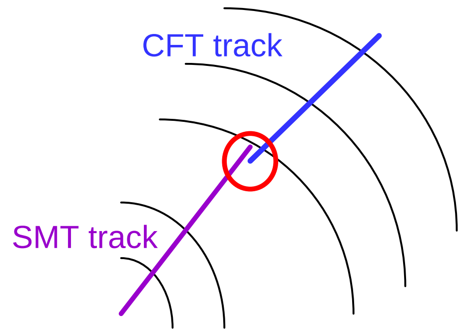
Very preliminary. Need to have a closer look.

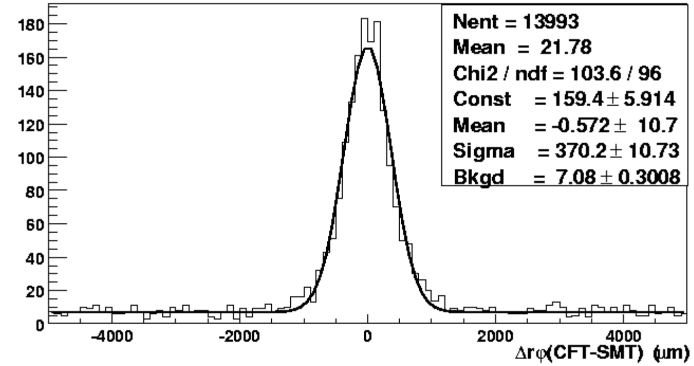
Expected depletion voltage



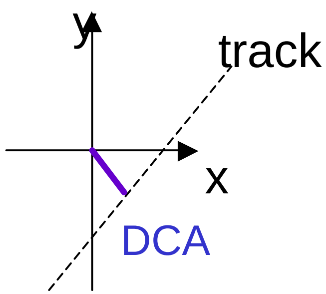
Results: Tracking and Vertexing (prelim.)

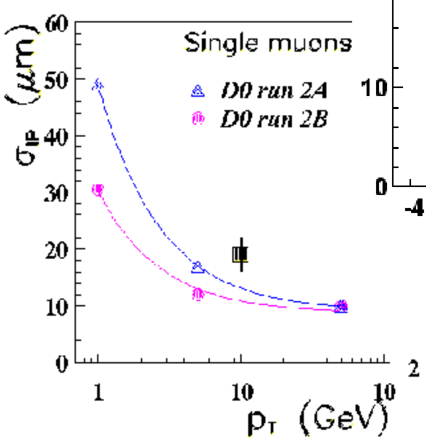
CFT-SMT track matching

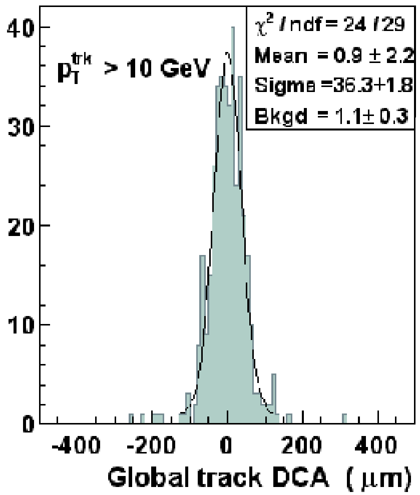




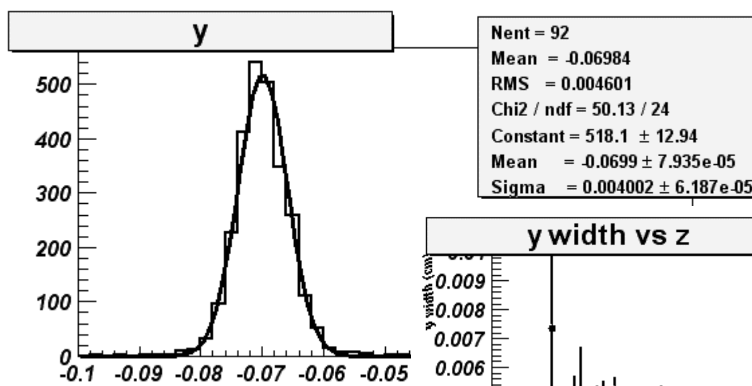
Impact parameter resolution

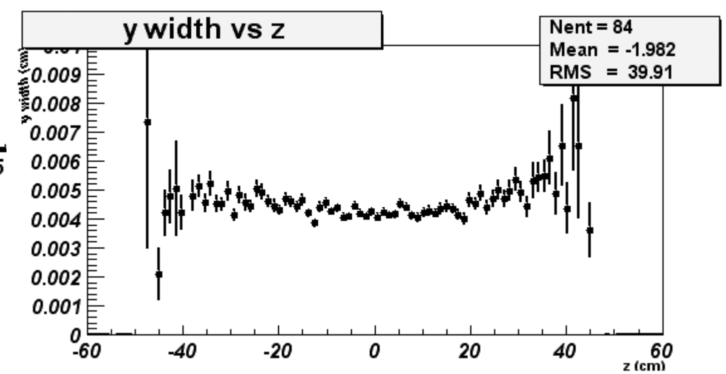






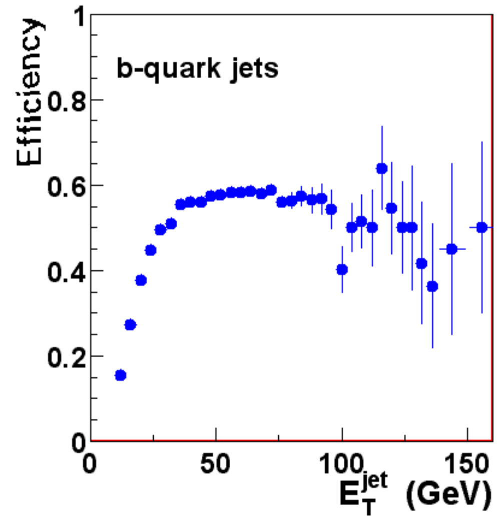
Vertex measurements

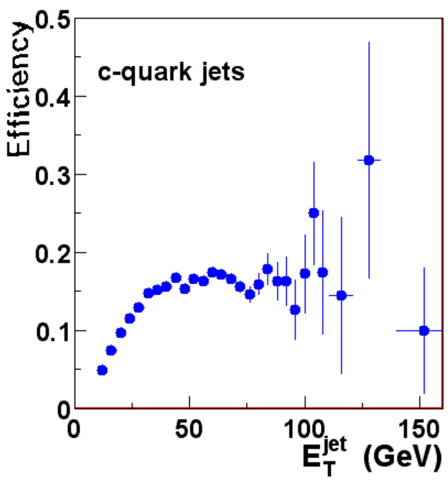


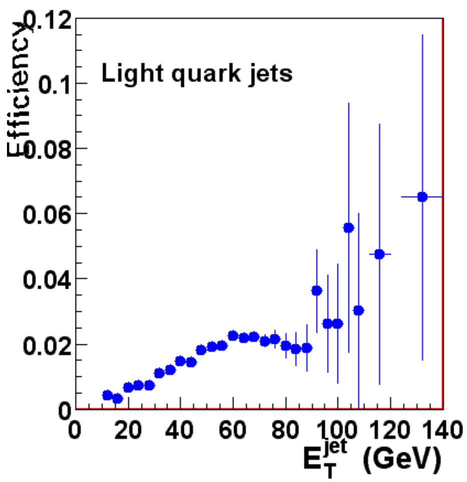


Results: b-tagging (preliminary)

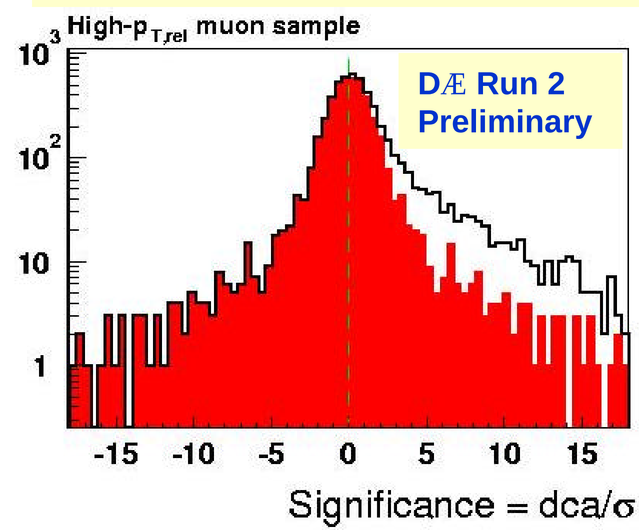
- Preliminary results indicate
  - b-tagging efficiency as high as 60% can be achieved
  - Mis-tagging rate for c-jets is less than 15 - 20% depending on E_T, while light quark rate can be kept at a few percent level





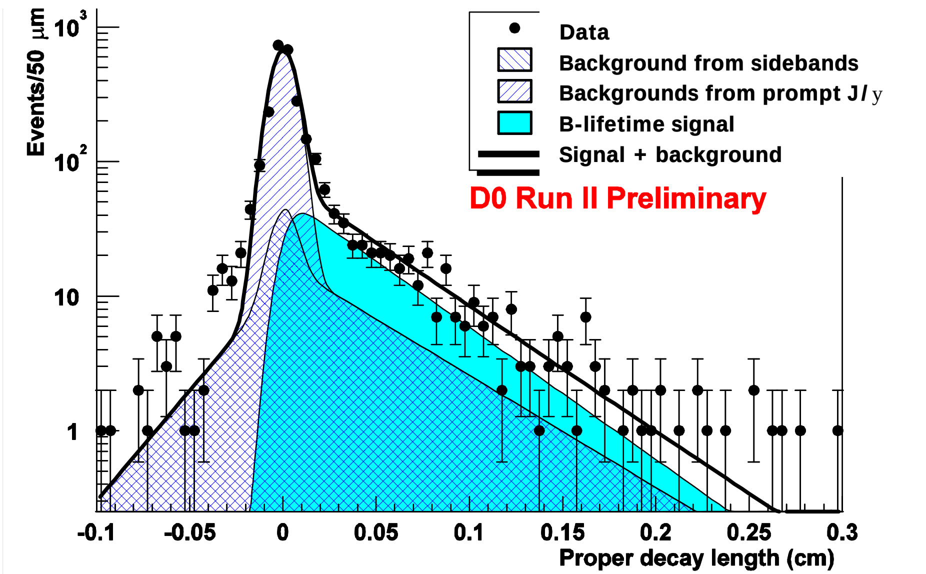


Tagging in μ+jet data sample: muon p_T^{rel} > 1.5 GeV wrt the jet



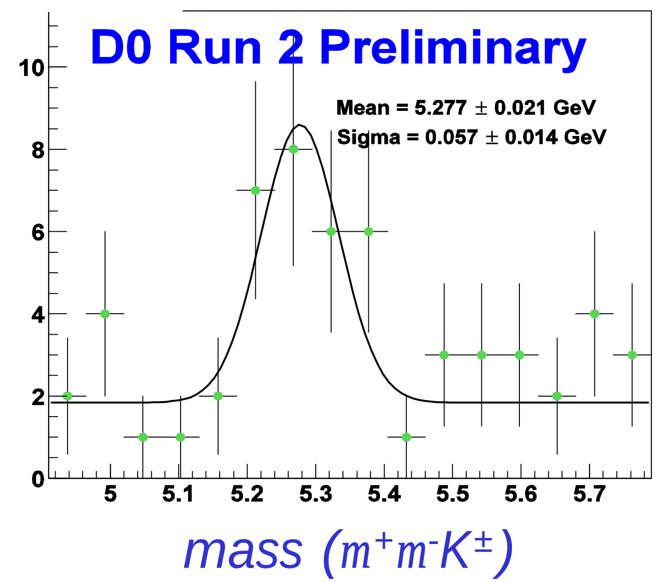
B - physics (preliminary)

Proper B decay length ($B \to J/\psi + X$)



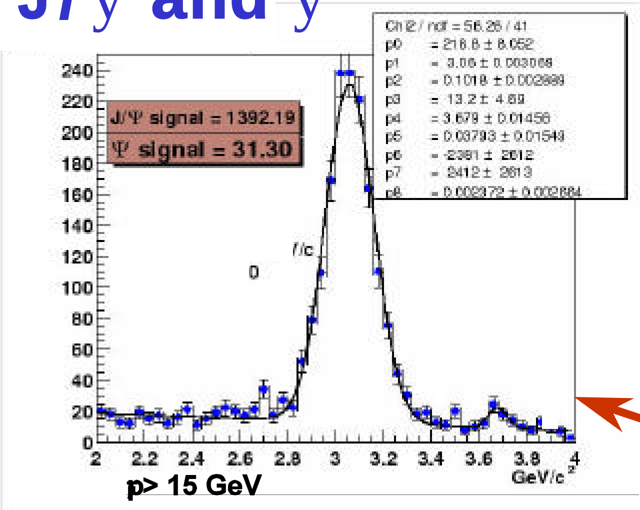
$B^{\pm} \to J/\psi\ K^{\pm}$

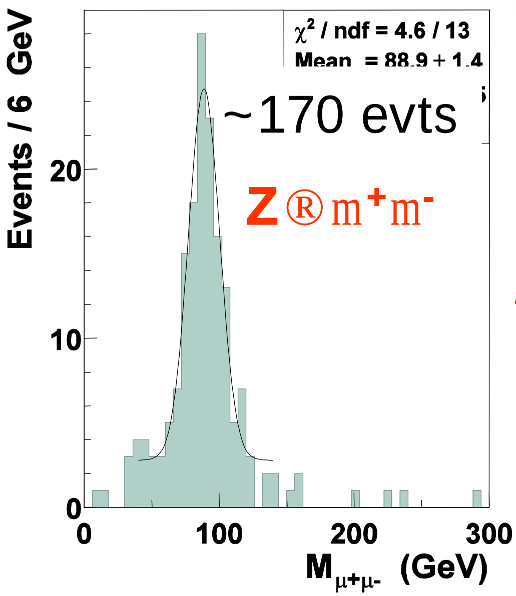
First time in DØ !



Physics with tracking (preliminary)

J/ψ and ψ'

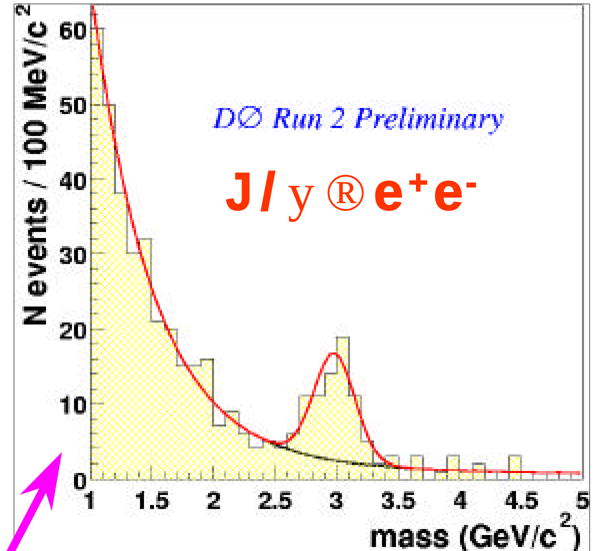


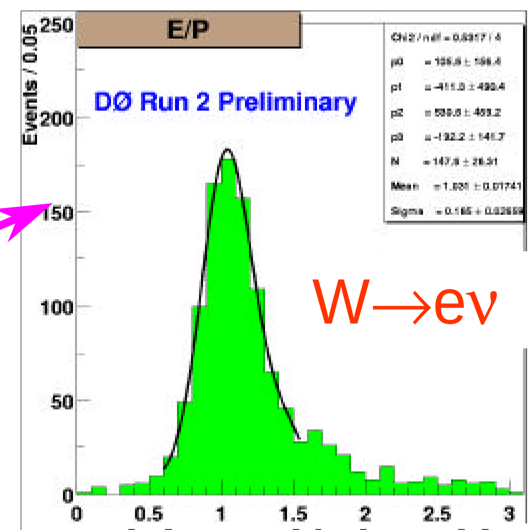


Combine tracking with other systems

Muon System

Calorimeter





E(cluster)/p(track)

Conclusions

- **Design/Production**
  - Experience with double-sided detectors has led to the decision to use single-sided silicon for the upgrade.
  - Should work towards simpler designs in the future. For example, using 6 different sensor types resulted in extensive logistical complications.
  - Had to overcome numerous vendor related problems for HDIs, Silicon Sensors, jumpers, low mass cables …
- **Assembly/Installation**
  - First alignment results show that the DØ SMT was assembled and installed very well.
  - The installation in the D0 detector went rather smoothly. The biggest challenge to overcome was the lack of real estate. The D0 detector, when first designed, was unfortunately not designed with a Silicon detector in mind

Conclusions

- **Commissioning and operation**
  - The SMT was the first major DØ Upgrade detector system fully operational for Run 2a.
  - We had our share of mishaps (IB PS, IB crate water leak, ...), but recovered from them.
  - 90% of the channels are functional, and most of the remaining channels will be debugged and should hopefully be recovered during the January 2003 shutdown.
  - Calibrations and first look at physics show that we understand our detector.
  - Altough the detector is close to being fully commissioned, some studies still need to be completed.

Partial to-do list

- Some studies to complete:
  - Pedestal shifts
    - where does it come from
    - how to suppress it
  - F-wedge excess noise:
    - where does it come from
    - how to suppress it
  - Bias currents:
    - study the effect of radiation
  - Effect of magnetic field on wire bonds

- Go to the next level of sophistication:
  - Online:
    - develop more monitoring tools
  - Offline:
    - alignment
    - clustering
    - tracking (efficiency, fully implement disks ...)
    - simulation

Conclusions

- **General**
  - Construction and commissioning of the SMT has been an adventure full of challenges. But thanks to the relentless efforts of many physicists, engineers and technicians, D0 has now a vertex detector to do physics with. Results start pouring ...
  - We had so much fun building this detector for run 2a that we are planning to build a completely new Silicon Microstrip detector for run 2b (see Kazu's talk)